(19) Eur päisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 809 351 A2

# (12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
**26.11.1997 Bulletin 1997/48**

(51) Int. Cl.[6]: **H03F 1/32**

(21) Application number: **97113589.2**

(22) Date of filing: **08.12.1993**

(84) Designated Contracting States:
**DE FR GB IT NL SE**

(30) Priority: **08.12.1992 JP 351747/92**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
**93119773.5 / 0 601 560**

(71) Applicant: **NEC CORPORATION**
**Tokyo (JP)**

(72) Inventor: **Kimura, Katsuji**
**Minato-ku, Tokyo (JP)**

(74) Representative:
**VOSSIUS & PARTNER**
**Siebertstrasse 4**
**81675 München (DE)**

Remarks:
This application was filed on 06 - 08 - 1997 as a divisional application to the application mentioned under INID code 62.

## (54) Differential amplifier circuit

(57) A differential amplifier circuit having an improved transconductance linearity, which includes a first to fourth unbalanced differential pairs of MOS transistors. In each differential pair, a ratio (W/L) of a gate-width W and a gate-length L of one transistor is different from that of the other transistor. Gates of the transistors having smaller ratios of the first and third pairs and gates of the transistors having larger ratios of the second and fourth pairs are coupled together to form one of differential input ends. Gates of the transistors having larger ratios of the first and third pairs and gates of the transistors having smaller ratios of the second and fourth pairs are coupled together to form the other of the input ends. Drains of the transistors having smaller ratios of the first and second pairs and drains of the transistors having larger ratios of the third and fourth pairs are coupled together to form one of differential output ends. Drains of the transistors having larger ratios of the first and second pairs and drains of the transistors having smaller ratios of the third and fourth pairs are coupled together to form the other of the output ends.

EP 0 809 351 A2

## Descripti n

The present invention relates to a differential amplifier circuit and more particularly, to a differential amplifier circuit to be formed on Complementary Metal Oxide Semiconductor (CMOS) integrated circuits or on bipolar integrated circuits, which has an improved transconductance linearity.

Fig. 1 shows an example of conventional differential amplifier circuits with a CMOS structure whose transconductance linearity is improved.

The differential amplifier circuit shown in Fig. 1 is composed of a first differential pair of MOS transistors M11 and M12 which are driven by a constant current source 51 (current: $I_0$) and a second differential pair of MOS transistors M13 and M14 which are driven by a constant current source 52 (current: $aI_0$, $a \neq 1$). The transistor M11 has the same ratio (W/L) between its gate length L and gate width W as that of the transistor M12, the transistor M13 has the same ratio (W/L) between its gate length L and gate width W as that of the transistor M14. When the transconductance parameters of the transistors M11 and M12 are both defined as $\beta$, the transconductance parameters of the transistors M13 and M14 are $b\beta$ where $b \neq 1$, respectively.

The transconductance parameter $\beta$ is expressed as

$$\beta = \mu(C_{OX}/2)(W/L) \tag{1}$$

where $\mu$ is the effective surface carrier mobility and $C_{OX}$ is a gate-oxide capacity per unit area.

In Fig. 1, the gates of the transistors M 11 and M14 coupled together and the gates of the transistors M 12 and M13 coupled together form differential input ends of the differential amplifier circuit. An input voltage $V_{in}$ is applied to the differential input ends.

The drains of the transistors M11 and M13 coupled together and the drains of the transistors M12 and M14 coupled together form differential output ends of the differential amplifier circuit.

The sources of the transistors M11 and M12 are connected in common to the constant current source 51 and the sources of the transistors M13 and M14 are connected in common to the constant current source 52.

Assuming that the transistors M11, M12, M13 and M14 are operating at their saturation regions, drain currents $I_{d11}$ and $I_{d12}$ of the transistors M11 and M12 are respectively expressed as the following equations (2-1) and (2-2) using the transconductance parameter $\beta$, the threshold voltage $V_{TH}$ of the transistors M11, M12, M13 and M14 and gate-source voltages $V_{GS11}$ and $V_{GS12}$ of the transistor M11 and M12.

$$I_{d11} = \beta(V_{GS11} - V_{TH})^2 \tag{2-1}$$

$$I_{d12} = \beta(V_{GS12} - V_{TH})^2 \tag{2-2}$$

The drain currents $I_{d11}$ and $I_{d12}$ satisfies the relationship as $I_{d11} + I_{d12} = I_0$.

Accordingly, the difference of the drain currents $I_{d11}$ and $I_{d12}$ is given as the following equations (3-1),(3-2) and (3-3).

$$I_{d11} - I_{d12} = \beta V_{in} \sqrt{(2I_0/\beta) - V_{in}^2} \quad (|V_{in}| \leq \sqrt{I_0/\beta}) \tag{3-1}$$

$$I_{d11} - I_{d12} = I_0 \quad (V_{in} \geq \sqrt{I_0/\beta}) \tag{3-2}$$

$$I_{d11} - I_{d12} = -I_0 \quad (V_{in} \leq -\sqrt{I_0/\beta}) \tag{3-3}$$

In the equations (3-1), (3-2) and (3-3), the input voltage $V_{in}$ satisfies the expression as $V_{in} = V_{GS11} - V_{GS12}$.

Drain currents $I_{d13}$ and $I_{d14}$ of the transistors M13 and M14 can be expressed as equations similar to the equations (2-1) and (2-2), respectively. Here, the drain currents $I_{d13}$ and $I_{d14}$ satisfies the relationship as $I_{d13} + I_{d14} = aI_0$, so that the difference of the drain currents $I_{d13}$ and $I_{d14}$ is expressed as the following equations (4-1),(4-2) and (4-3), where $a < (a/b) < 1$.

$$I_{d3} - I_{d4} = b\beta V_{in} \sqrt{(2aI_0)/(b\beta) - V_{in}^2} \quad (|V_{in}| \leq \sqrt{(aI_0)/(b\beta)}) \tag{4-1}$$

$$I_{d3} - I_{d4} = aI_0 \quad (|V_{in}| \geq \sqrt{(aI_0)/(b\beta)}) \tag{4-2}$$

$$I_{d3} - I_{d4} = -aI_0 \quad (|V_{in}| \leq -\sqrt{(aI_0)/(b\beta)}) \tag{4-3}$$

The differential output current $\Delta I$ of the differential amplifier circuit shown in Fig. 1 is given as the following equations (5-1), (5-2) and (5-3).

$$\Delta I = (I_{d1} + I_{d4}) - (I_{d2} + I_{d3}) \quad (5\text{-}1)$$
$$= (I_{d1} - I_{d2}) - (I_{d3} - I_{d4})$$
$$= -\beta V_{in} [\sqrt{(2I_0/\beta) - V_{in}^2} - b\sqrt{(2aI_0)/(b\beta) - V_{in}^2}] \; (|V_{in}| \le \sqrt{(2aI_0)/(b\beta)})$$

$$\Delta I = \beta V_{in} \sqrt{(2I_0)/\beta - V_{in}^2} - aI_0 \, sgn(V_{in}) \; (\sqrt{(aI_0)/(b\beta)} \le |V_{in}| \le \sqrt{I_0/\beta}) \quad (5\text{-}2)$$

$$\Delta I = (1 - a) I_0 \, sgn(V_{in}) \; (|V_{in}| \le \sqrt{I_0/\beta}) \quad (5\text{-}3)$$

The differential output current ΔI shown as the equations (5-1), (5-2) and (5-3) is differentiated by the input voltage $V_{in}$. To make the transconductance substantially constant in the equations (5-1), (5-2) and (5-3), the values of the equation obtained by the differentiation when $V_{in} = 0$ and $|V_{in}| = \{(aI_0)/(b\beta)\}^{1/2}$ are required to be equal to each other. Therefore, the following relationship has to be satisfied as

$$1 = (b \cdot b^{1/2})/a^{1/2} \quad (6)$$

Fig.2 shows the transconductance characteristics of the conventional differential amplifier circuit shown in Fig. 1 with the constants **a** and **b** as parameters. In Fig. 2, it is seen that the fluctuation of the transconductance is limited to 3 % or less in the input voltage range of $|V_{in}| \le 0.7(I_0/\beta)^{1/2}$.

Fig. 3 shows another example of the conventional differential amplifier circuits whose transconductance is good in linearity, which is disclosed by A. Nedungadi and T. R. Viswanathan in IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, Vol. CAS-31, No.10, pp. 891-894, October 1984, entitled "Design of Linear CMOS transconductance Elements".

In this paper, they supposed that when the gate lengths of two MOS transistors forming each unbalanced differential pair were equal to each other, the differential amplifier circuit which are composed of two of the unbalanced differential pairs whose output ends are cross-coupled would have improved linearity of the transconductance if a ratio of the gate widths of the MOS transistors forming each unbalanced differential pair were larger. Then, they obtained a conclusion through the SPICE simulation in which the ratio of the gate widths are 10 and 20 that the ratio of the gate widths was required to be 10 or more.

Additionally, they thought that the above-mentioned conclusion is not practical since such a large ratio as 10 or more leads to a large chip area. Therefore, they proposed the differential amplifier circuit shown in Fig. 3.

In Fig. 3, there is provided a "Cross-Coupled Quad Cell" formed of MOS transistors M21, M22, M23 and M24 as a squaring circuit thereby to improve the transconductance linearity of a balanced differential pair formed of MOS transistors M26 and M27 having the same gate-width to gate-length ratio (W/L).

The MOS transistors M21 and M22 compose a first differential pair and the MOS transistors M23 and M24 compose a second differential pair. The first differential pair is driven by a constant current source 61 which is connected to the common-connected sources of the transistors M21 and M22 and generates a constant current (n+1)I. The second differential pair is driven by a constant current source 62 which is connected to the common-connected sources of the transistors M23 and M24 and generates a constant current (n+1)I.

The transconductance parameters of the transistors M21 and M22 are $k_0$ and those of the transistors M23 and M24 are **n** times as much as $k_0$, or $nk_0$. The MOS transistor with the transconductance parameter $nk_0$ is generally realized by **n** in number of the unit transistors with the transconductance parameter $k_0$ which are connected in parallel.

The MOS transistors M26 and M27 whose sources are connected in common at a point B compose a differential pair, which is driven by a constant current source 63 generating a constant current aI. The constant current source 63 is connected to the differential pair at the point B and generates a constant current aI. The transconductance parameters of the transistors M26 and M27 are $k_0$.

The gates of the transistors M26, M21 and M23 are coupled together to be applied with a first input voltage $V_1$. The gates of the transistors M27, M22 and M24 are coupled together to be applied with a second input voltage $V_2$.

The drains of the transistors M23 and M24 are connected in common to a voltage source (voltage: $V^+$). The drains of the transistors M21 and M22 are coupled together at a point A, and between the drains thus coupled together and the voltage source, there is provided with a constant current source 64 which generates a constant current aI. An MOS transistor 25 whose drain and gate are connected to each other is provided between the points A and B. The transistor M25 serves as a current level shifter for shifting the current level at the point A to that at the point B.

MOS transistors M28 and M29 compose a current mirror circuit serving as an active load of the differential amplifier circuit. An output current i of the differential amplifier circuit is derived from the drain of the transistor M29.

In the conventional differential amplifier circuit shown in Fig. 3, in the range of $|x| \le (n+1)^{1/2}$ where $V_1 - V_2 = v$ and $x = v/(I/k_0)^{1/2}$, the drain current $I_{D21}$, $I_{D22}$, $I_{D23}$ and $I_{D24}$ of the transistors M21, M22, M23 and M24 are expressed as the following equations (7-1), (7-2), (7-3) and (7-4), respectively.

$$I_{D21}=I[1+\gamma x^2+(\alpha/2)x(1-\beta x^2)^{1/2}] \quad (7\text{-}1)$$

$$I_{D22}=I[1+\gamma x^2+(\alpha/2)x(1-\beta x^2)^{1/2}] \quad (7\text{-}1)$$

$$I_{D23}=I[n-\gamma x^2+(\alpha/2)x(1-\beta x^2)^{1/2}] \quad (7\text{-}3)$$

$$I_{D24}=I[n-\gamma x^2+(\alpha/2)x(1-\beta x^2)^{1/2}] \quad (7\text{-}4)$$

In the equations (7-1), (7-2), (7-3) and (7-4), $\alpha$, $\beta$ and $\gamma$ are defined as the following expressions (8-1), (8-2) and (8-3), respectively.

$$\alpha=4n/(n+1) \quad (8\text{-}1)$$

$$\beta=n/(n+1)^2 \quad (8\text{-}2)$$

$$\gamma=n(n-1)/(n+1)^2 \quad (8\text{-}3)$$

The drain current $I_{D21}$, $I_{D22}$, $I_{D23}$ and $I_{D24}$ and the constant currents $(n+1)I$ of the current sources 61 and 62 satisfy the following relationship as

$$I_{D21} + I_{D24} = I_{D22} + I_{D23} = (n+1)I \quad (9)$$

Accordingly, the sum $(I_{D21} + I_{D22})$ of the drain currents $I_{D21}$ and $I_{D22}$ can be expressed as the following equation (10) and the drain currents $I_{D25}$ of the transistor M25 can be expressed as the following equation (11).

$$I_{D21} + I_{D22} = 2I[1+\gamma x^2] = 2I + \{2n(n-1)/(n+1)^2\}Ix^2 \quad (10)$$

$$I_{D25} = aI - (I_{D21} + I_{D22}) \quad (11)$$

Here, the current of the balanced differential pair of the transistors M26 and M27 is defined as $I_0$, then the output current is expressed as the following equation (12).

$$i = I_{D6} - I_{D7} = k'V\{2I_0/k') - V^2\}^{1/2} \ (|v| \le (I_0/k')^{1/2}) \quad (12)$$

The current $I_0$ satisfies the relationship as

$$\begin{aligned} I_0 &= aI - I_{D5} = I_{D1} + I_{D2} \\ &= 2I + [\{2Kn(n-1)\}/(n+1)^2]v^2 \end{aligned} \quad (13)$$

Thus, if the equation (13) is substituted into the equation (12), the output current i can be expressed as

$$i = k'v\sqrt{\frac{4I}{k'} + \{\frac{2n(n-1)k_0}{(n+1)^2 k'} - 1\}v^2} \quad (14)$$

If the relationship between $k_0$ and k' is selected as the following expression (15), the output current i is obtained as the following equation (16).

$$k' = \{2n(n-1)/(n+1)^2\}k_0 \quad (15)$$

$$\begin{aligned} i &= 2v\sqrt{Ik'} \\ &= \frac{2\sqrt{2n(n-1)\ Ik_0}}{n+1}v \end{aligned} \quad (16)$$

It is seen from the equation (16) that the differential amplifier circuit shown in Fig. 3 has a very good transconductance linearity.

Fig. 4 shows still another example of the conventional differential amplifier circuits to be formed on bipolar integrated circuits, which is disclosed by M. Koyama, H. Tanimoto and S. Mizoguchi in IEEE 1989 Custom Integrated Circuits Conference, pp. 25.2.1 - 25.2.4, entitled "10.7 MHz Continuous-Time Bandpass filter Bipolar IC".

In Fig. 4, bipolar transistors Q11 and Q12 compose a first differential pair which is driven by a constant current source 71 (current: $I_0$). Emitters of the transistors Q11 and Q12 are connected in common to the current source 71. Bipolar transistors Q13 and Q14 compose a second differential pair which is driven by a constant current source 72 (current: $I_0$). Emitters of the transistors Q13 and Q14 are connected in common to the current source 72.

Collectors of the transistors Q11 and Q13 coupled together and collectors of the transistors Q12 and Q14 coupled together form differential output ends of the differential amplifier circuit. Bases of the transistors Q11 and Q12 form differential input ends of the differential amplifier circuit to be applied with an input voltage $V_{in}$.

A direct current (DC) voltage source 73 (Voltage: $V_k$) is provided between the bases of the transistors Q11 and Q13 and a DC voltage source 74 (Voltage: $V_k$) is provided between the bases of the transistors Q14 and Q12. Thus, bias voltages $V_k$ are respectively applied to the bases of the transistors Q12 and Q13 with their negative ends at the bases of the transistors Q11 and Q14.

An electric current (emitter current) $I_E$ of a p-n junction diode forming a bipolar transistor can be expressed by the following equation (17), where $I_s$ is the saturation current, $k_B$ is Boltzmann's constant, q is the unit electron charge, $V_{BE}$ is a base-to-emitter voltage of the transistor and T is absolute temperature.

$$I_E = I_S [\exp\{(qV_{BE})/(k_BT)\} - 1] \quad (17)$$

Here, if the thermal voltage $V_T$ is defined as $V_T = kT/q$, as $V_{BE} >> V_T$, when $\exp(V_{BE}/V_T) >> 1$ in the equation (17), the emitter current $I_E$ can be approximated as follows;

$$I_E \fallingdotseq I_S \exp(V_{BE}/V_T) \quad (18)$$

As a result, collector currents $I_{C11}$ and $I_{C12}$ of the transistors Q11 and Q12 can be obtained as follows:
Base-to-emitter voltages of the transistors Q11 and Q12 are expressed as

$$V_{BE11} = V_T \ln(I_{C11}/Is) \quad (19\text{-}1)$$

and

$$V_{BE12} = V_T \ln(I_{C12}/Is) \quad (19\text{-}2)$$

Here, the difference between the voltages $V_{BE11}$ and $V_{BE12}$ is defined as $V_1$, or $V_{BE11} - V_{BE12} = V_1$. Then, the sum of the collector currents $I_{C11}$ and $I_{C12}$ is expressed as $I_{C11} + I_{C12} = \alpha_F I_E$ where $\alpha_F$ is the DC common-base current gain factor. Therefore, the collector currents $I_{C11}$ and $I_{C12}$ can be given as the following equations (20-1) and (20-2), respectively.

$$I_{C11}=(\alpha_F I_0)/\{1+\exp(-V_1/V_T)\} \quad (20\text{-}1)$$

$$I_{C12}=(\alpha_F I_0)/\{1+\exp(V_1/V_T)\} \quad (20\text{-}2)$$

From the equations (20-1) and (20-2), the difference $\Delta I_1$ between the collector currents $I_{C11}$ and $I_{C12}$ is given as

$$\Delta I_1 = I_{C11} - I_{C12} = \alpha_F I_0 \tanh\{V_1/(2V_T)\} \quad (21)$$

The transconductance $G_{m1}$ is expressed by differentiating the difference $\Delta I_1$ by the voltage $V_1$ as the following equation (22).

$$G_{m1} = d(\Delta I_1)/dV_1 = \{(\alpha_F I_0)/(2V_T)\}[1/\{\cosh^2(V_1/(2V_T))\}] \quad (22)$$

In the equation (22), the difference $V_1$ between the base-to-emitter voltages $V_{BE11}$ and $V_{BE12}$ is defined as $V_1 = V_{in} - V_k$ where $V_k$ is the offset bias voltage described above.

With the second differential pair of the transistors Q13 and Q14, similarly, the difference $\Delta I_2$ between the collector currents $I_{C13}$ and $I_{C14}$ of the transistors Q13 and Q14 can be expressed as the following equation (23).

$$\Delta I_2 = I_{C13} - I_{C14} = \alpha_F I_0 \tanh\{V_2/(2V_T)\} \quad (23)$$

In the equation (23), the difference $V_2$ between the base-to-emitter voltages $V_{BE13}$ and $V_{BE14}$ is defined as $V_2 = V_{in} - V_k$, so that the sum $\Delta I$ of the current differences $\Delta I_1$ and $\Delta I_2$ can be given by the following equation (24).

$$\begin{aligned}\Delta I &= \Delta I_1 + \Delta I_2 \\ &= \alpha_F I_0 [\tanh\{(V_{in} - V_k)/(2V_T)\} + \tanh\{(V_{in} + V_k)/(2V_T)\}]\end{aligned} \quad (24)$$

The sum $G_m$ of the transconductances $G_{m1}$ and $G_{m2}$ of the first and second differential pairs can be given by the following equation (25).

$$\begin{aligned}G_m &= G_{m1} + G_{m2} \\ &= d(\Delta I_1)/dV_{in} + d(\Delta I_2)/dV_{in} \\ &= \{(\alpha_F I_0)/(2V_T)\} \times \\ &\quad [[1/\cosh^2\{(V_{in} - V_k)/(2V_T)\}] + [1/\cosh^2\{(V_{in} + V_k)/(2V_T)\}]]\end{aligned} \quad (25)$$

The transconductance $G_{m1}$ in the equation (22) shows the maximally flat characteristic when $V_K = 1.3137\ V_T$. Fig. 5 shows the transconductance characteristics of the differential amplifier circuit. It is seen from Fig. 5 that the fluctuation of the transconductance is limited to -1 % or less when $|V_{in}| \leq V_T$.

The conventional differential amplifier circuits described above have the following problems. With the differential amplifier circuit shown in Fig. 1, since the circuit has the transconductance fluctuation about 3 %, it cannot be employed to applications requiring the fluctuation less than 3 %, which means that application fields of the circuit is narrow. In addition, since the differential output current is expressed as the difference between the drain current difference, the current efficiency with respect to the driving currents is low.

With the conventional differential amplifier circuit shown in Fig. 3, the differential pair composing the squaring circuit is realized by an MOS transistor with the transconductance parameter $k_0$ and n in number of the MOS transistors with the transconductance parameter $k_0$ which are connected in parallel. Therefore, the chip occupation area is expanded and the current consumption increases due to a large number of elements.

For example, choosing $k' = k_0/2$ in the equation (15), we get $n = 1 + 2/3^{1/2} \fallingdotseq 2.155$. Therefore, to obtain a very good transconductance linearity, each of the unbalanced differential pairs must be composed of 431 in number of unit transistors and 200 in number of the unit transistors, which requires a very large chip occupation area. Thus, the conventional differential amplifier circuit shown in Fig. 3 is not practical.

With the differential amplifier circuit shown in Fig. 4, the input voltage range is not wide to be satisfied.

Accordingly, an object of the present invention is to provide a differential amplifier circuit in which an improved transconductance linearity can be obtained and its circuit configuration is simple without enlarging its circuit scale.

Another object of the present invention is to provide a differential amplifier circuit in which the current efficiency can be improved.

Still another object of the present invention is to provide a differential amplifier circuit which has a substantially linear transconductance in a wider range than the conventional one.

These objects are achieved by the features of the independent claims.

A differential amplifier circuit according to a first aspect of the present invention includes a first differential pair of first and second transistors, a second differential pair of third and fourth transistors and a third differential pair of fifth and sixth transistors.

Bases of the first and fifth transistors coupled together and bases of the fourth and sixth transistors coupled together form differential input ends. Collectors of the first, third and fifth transistors coupled together and drains of the second, fourth and sixth transistors coupled together form differential output ends.

A first DC voltage is applied across the bases of the first and third transistors and a second DC voltage is applied across the bases of the second and fourth transistors.

With the differential amplifier circuit of the first aspect, the input voltage is applied across the input ends of the first differential pair together with the second DC voltages as an offset bias voltage, the input voltage is applied across the input ends of the second differential pair together with the first DC voltages as an offset bias voltage, and the input voltage is applied directly across the input ends of the third differential pair.

Therefore, an improved transconductance linearity can be obtained and as a result, the input voltage range can be

expanded.

Additionally, improved high-frequency characteristics can be given since each differential pair is formed of two minimum unit transistors.

A differential amplifier circuit according to a second aspect of the present invention includes a first differential pair of first and second transistors, a second differential pair of third and fourth transistors, a third differential pair of fifth and sixth transistors, and a fourth differential pair of seventh and eighth transistors.

Bases of the first and fifth transistors coupled together and bases of the fourth and eighth transistors coupled together form differential input ends. Collectors of the first, third, fifth and seventh transistors coupled together and collectors of the second, fourth, sixth and eighth transistors coupled together form differential output ends.

A first DC voltage is applied across the bases of the first and third transistors, a second DC voltage is applied across the bases of said second and fourth transistors, a third DC voltage is applied across the bases of the fifth and seventh transistors, and a fourth DC voltage is applied across the bases of the sixth and eighth transistors.

With the differential amplifier circuit of the second aspect the input voltage is applied across the input ends of the first differential pair together with the second DC voltages as an offset bias voltage, the input voltage is applied across the input ends of the second differential pair together with the first DC voltages as an offset bias voltage, the input voltage is applied across the input ends of the third differential pair together with the fourth DC voltages as an offset bias voltage, and the input voltage is applied across the input ends of the fourth differential pair together with the third DC voltages as an offset bias voltage.

Therefore, similar to the circuit of the first aspect an improved transconductance linearity can be obtained and as a result, the input voltage range can be expanded.

Additionally, improved high-frequency characteristics can be given since each differential pair is formed of two minimum unit transistors.

Fig. 1 is a circuit diagram of a conventional differential amplifier circuit.

Fig. 2 shows a transconductance characteristic of the conventional differential amplifier circuit shown in Fig. 1.

Fig. 3 is a circuit diagram of another conventional differential amplifier circuit.

Fig. 4 is a circuit diagram of still another conventional differential amplifier circuit.

Fig. 5 shows a transconductance characteristic of the conventional differential amplifier circuit shown in Fig. 4.

Fig. 6 is a circuit diagram of a first differential amplifier circuit.

Fig. 7 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 6.

Fig. 8 is a circuit diagram of a second differential amplifier circuit.

Fig. 9 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 8.

Fig. 10 is a circuit diagram of a third differential amplifier circuit.

Fig. 11 shows an output characteristic of the differential amplifier circuit shown in Fig. 10.

Fig. 12 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 10.

Fig. 13 is a circuit diagram of a differential amplifier circuit according to a first embodiment of the present invention.

Fig. 14 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 13 in which $V_K = 2.634\ V_T$ and (1/a) = (4/3).

Fig. 15 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 13 in which $V_K = 2.06344\ V_T$ and (1/a) = 1.5625.

Fig. 16 is a circuit diagram of a differential amplifier circuit according to second embodiment of the present invention.

Fig. 17 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 16 in which $V_{K1} = 1.2\ V_T$, $V_{K2} = 3.834\ V_T$ and a = 1.3.

Fig. 18 shows a transconductance characteristic of the differential amplifier circuit shown in Fig. 16 in which $V_{K1} = 0.70814\ V_T$, $V_{K2} = 2.59546\ V_T$ and (1/a) = 1.82532.

The embodiments, which will be described below referring to Figs. 6 to 12 are claimed and described in the parent application EP 93 11 9773.5

Fig. 6 shows a first differential amplifier circuit.

In Fig. 6, N-channel MOS transistors M1 and M2 compose a first differential pair which is driven by a constant current source 1 whose current value is $I_0$. N-channel MOS transistors M3 and M4 compose a second differential pair which is driven by a constant current source 2 whose current value is $I_0$. The first and second differential pairs form a first combined differential pair.

N-channel MOS transistors M5 and M6 compose a third differential pair which is driven by a constant current source 3 whose current value is $aI_0$ where $a \neq 1$. N-channel MOS transistors M7 and M8 compose a fourth differential pair which is driven by a constant current source 4 whose current value is $aI_0$. The third and fourth differential pairs form a second combined differential pair.

In the first combined differential pair, a ratio (W/L) of a gate-width W and a gate-length L of the transistor M2 is K times as much as that of the transistor M1 where $K \neq 1$. A ratio (W/L) of the transistor M3 is K times as much as that of the transistor M4. The ratios (W/L) of the transistors M1 and M4 are equal to each other.

Gates of the transistor M1 whose relative ratio is 1 and the transistor M3 whose relative ratio is K are coupled together and gates of the transistor M4 whose relative ratio is 1 and the transistor M2 whose relative ratio is K are coupled together. Drains of the transistors M1 and M4 whose relative ratios are 1 are coupled together and drains of the transistors M2 and M3 whose relative ratios are K are coupled together.

In the second combined differential pair, a ratio (W/L) of a gate-width W and a gate-length L of the transistor M6 is K' times as much as that of the transistor M5 where $K' \neq 1$. A ratio (W/L) of the transistor M7 is K' times as much as that of the transistor M8. The ratios (W/L) of the transistors M5 and M8 are equal to each other.

The ratios (W/L) of the transistor M5 and M8 are b times as much as those of the transistors M1 and M4 where $b' \neq 1$. Therefore, the ratios (W/L) of the transistors M6 and M7 are K'b times as much as those of the transistors M1 and M4.

Gates of the transistor M5 whose relative ratio is 1 and the transistor M7 whose relative ratio is K' are coupled together and gates of the transistor M8 whose relative ratio is 1 and the transistor M6 whose relative ratio is K' are coupled together. Drains of the transistors M5 and M8 whose relative ratios are 1 are coupled together and drains of the transistors M6 and M7 whose relative ratios are K' are coupled together.

The gates coupled of the transistors M1 and M3 and the gates coupled of the transistors M5 and M7 are coupled together to form one of differential input ends. The gates coupled of the transistors M2 and M4 and the gates coupled of the transistors M6 and M8 are coupled together to form the other of the differential input ends. An input voltage $V_{in}$ is applied across the differential input ends thus formed.

The drains coupled of the transistors M1 and M4 and the drains coupled of the transistors M6 and M7 are coupled together to form one of differential output ends. The drains coupled of the transistors M2 and M3 and the drains coupled of the transistors M5 and M8 are coupled together to form the other of the differential output ends.

In Fig. 6, $\beta$ indicates the transconductance parameters of the transistors M1 and M4. The transistors M1 to M8 have the transconductance parameters as shown in Fig. 6, respectively.

Next, the operation of the differential amplifier circuit is shown below.

In the first combined differential pair formed of the transistors M1 to M4, when gate-to-source voltages of the transistors M1, M2, M3 and M4 are expressed as $V_{GS1}$, $V_{GS2}$, $V_{GS3}$ and $V_{GS4}$ respectively, the threshold voltages of the transistors are as $V_{TH}$, drain currents $Id_{d1}$, $I_{d2}$, $I_{d3}$ and $I_{d4}$ of the transistors M1, M2, M3 and M4 can be expressed as the following equations (26-1), (26-2), (26-3) and (26-4), respectively.

$$I_{d1} = \beta(V_{GS1}-V_{TH})^2 \quad (26\text{-}1)$$

$$I_{d2} = K\beta(V_{GS2}-V_{TH})^2 \quad (26\text{-}2)$$

$$I_{d3} = K\beta(V_{GS3}-V_{TH})^2 \quad (26\text{-}3)$$

$$I_{d4} = \beta(V_{GS4}-V_{TH})^2 \quad (26\text{-}4)$$

The drain currents $Id_{d1}$, $I_{d2}$, $I_{d3}$ and $I_{d4}$ and the constant currents $I_0$ of the current sources 1 and 2 have the following relationship (27) and the gate-to-source voltages $V_{GS1}$, $V_{GS2}$, $V_{GS3}$ and $V_{GS4}$ and the input voltage $V_{in}$ have the following relationship (28).

$$I_{d1} + I_{d2} = I_{d3} + I_{d4} = I_0 \quad (27)$$

$$V_{GS1} - V_{GS2} = V_{GS4} - V_{GS3} = V_{in} \quad (28)$$

Therefore, the difference of the drain currents $Id_{d1}$ and $I_{d2}$ are given as the following expressions (29-1), (29-2) and (29-3), and the difference of the drain currents $Id_{d3}$ and $I_{d4}$ are given as the following expressions (30-1), (30-2) and (30-3).

$$I_{d1} - I_{d2} = \frac{\{1 - (1/K)\}[\{1 + (1/K)\} I_0 - 2\beta V_{in}^2\}}{\{1 + (1/K)\}^2} + \frac{\beta V_{in}(4/\sqrt{K}) \sqrt{\{1 + (1/K)\}(I_0/\beta) - V_{in}^2}}{\{1 + (1/K)\}^2} \quad (29\text{-}1)$$

$$\left(-\sqrt{I_0/\beta} \leq V_{in} \leq \sqrt{I_0/(K\beta)}\right)$$

$$I_{d1} - I_{d2} = I_0 \left(V_{in} \geq \sqrt{I_0/(K\beta)}\right) \quad (29\text{-}2)$$

$$I_{d1} - I_{d2} = -I_0 \left(V_{in} \leq -\sqrt{I_0/\beta}\right) \quad (29\text{-}3)$$

$$I_{d3} - I_{d4} = \frac{\{1 - (1/K)\}[\{1 + (1/K) I_0 - 2\beta V_{in}^2\}]}{\{1 + (1/K)\}^2} + \frac{\beta V_{in}(4/\sqrt{K}) \sqrt{\{1 + (1/K)\}(I_0/\beta) - V_{in}^2}}{\{1 + (1/K)\}^2} \quad (30\text{-}1)$$

$$\left(-\sqrt{I_0/(K\beta)} \leq V_{in} \leq \sqrt{I_0/\beta}\right)$$

$$I_{d3} - I_{d4} = I_0 \left(V_{in} \geq \sqrt{I_0/\beta}\right) \quad (30\text{-}2)$$

$$I_{d3} - I_{d4} = -I_0 \left(V_{in} \leq -\sqrt{I_0/(K\beta)}\right) \quad (30\text{-}3)$$

Accordingly, the differential output current $\Delta I_1$ of the first combined differential pair is given as the following expressions (31-1), (31-2) and (31-3).

$$\Delta I_1 = ( I_{d1} + I_{d3} ) - ( I_{d2} + I_{d4} )$$
$$= ( I_{d1} - I_{d2} ) + ( I_{d3} - I_{d4} )$$
$$= \frac{(8/\sqrt{K})\ \beta\ V_{in} \sqrt{\{ 1 + (1/K) \}(I_0/\beta) - V_{in}^2}}{\{1 + (1/K)\}^2} \qquad (31\text{-}1)$$
$$\left( |V_{in}| \leq \sqrt{I_0 / (K\beta)} \right)$$

$$\Delta I_1 = (4/\sqrt{K})\ \beta\ V_{in} \frac{\sqrt{\{1 + (1/K)\}(I_0/\beta) - V_{in}^2}}{\{1 + (1/K)\}^2}$$
$$+ \frac{2\{1 - (1/K)\}\ \beta\ V_{in}^2}{\{1 + (1/K)\}^2}\ sgn\ ( V_{in} ) \qquad (31\text{-}2)$$
$$+ \frac{2(1/K)}{1+(1/K)}\ I_0\ sgn\ ( V_{in} )$$
$$\left( \sqrt{I_0 / (K\beta)} \leq |V_{in}| \leq \sqrt{I_0/\beta} \right)$$

$$\Delta I_1 = 2 I_0\ sgn(V_{in})\ (|V_{in}| \geq \sqrt{I_0/\beta}) \qquad (31\text{-}3)$$

Differentiating the differential output current $\Delta I_1$ in the expressions (31-1), (31-2) and (31-3) by the input voltage $V_{in}$ leads the transconductance as shown in the following expressions (32-1), (32-2) and (32-3).

$$\frac{d\,(\,\Delta I_1\,)}{d\,V_{in}} = \frac{8K\sqrt{\beta\,I_0}}{(K+1)\,\sqrt{1+K}}\,[\,\sqrt{1-[V_{in}^2/\{\,(1+(1/K)\,)\,(I_0/\beta)\,\}}\,] - \frac{V_{in}^2/\,[\{\,1+(1/K)\}(I_0/\beta)\,]}{\sqrt{1+[\,V_{in}^2/\,[\{\,1+(1/K)\}(I_0/\beta)\,]}}\,] \quad (32\text{-}1)$$

$$(|\,V_{in}\,| \leq \sqrt{I_0/(K\beta)}\,)$$

$$\frac{d\,(\,\Delta I_1\,)}{d\,V_{in}} = \frac{4K\sqrt{\beta\,I_0}}{(K+1)\,\sqrt{1+K}}\,[\sqrt{1-[V_{in}^2/\{1+(1/K)\}(I_0/\beta)\,]} - \frac{V_{in}^2/\,[\{\,1+(1/K)\}(I_0/\beta)\,]}{\sqrt{1\,+\,V_{in}^2/\,[\{\,1+(1/K)\}(I_0/\beta)\,]}}\,] + \frac{4\{1-(1/K)\,\beta\,V_{in}}{\{1+(1/K)\}^2} \quad (32\text{-}2)$$

$$(\sqrt{I_0/(K\beta)} \leq |\,V_{in}\,| \leq \sqrt{I_0/\beta}\,)$$

$$\frac{d\,(\Delta I_1)}{d\,V_{in}} = 0\ (|\,V_{in}\,| \geq \sqrt{I_0/\beta}) \quad (32\text{-}3)$$

Similarly, in the second combined differential pair formed of the transistors M5 to M8, the differential output current $\Delta I_2$ of the second combined differential pair is given as the following expressions (33-1), (33-2) and (33-3) and the transconductance is given as the following expressions (34-1), (34-2) and (34-3).

$$\Delta I_2 = ( I_{d5} - I_{d6} ) + ( I_{d7} - I_{d8} )$$

$$= \frac{(8/\sqrt{K'})\, b\beta\, V_{in}\sqrt{\{1 + (1/K')\}\{(aI_0)/(b\beta)\} - V_{in}^2}}{\{1 + (1/K')\}^2} \qquad (33\text{-}1)$$

$$(|V_{in}| \leq \sqrt{(aI_0)/(K'b\beta)})$$

$$\Delta I_2 = \frac{(4/\sqrt{K'})\, b\beta\, V_{in}\sqrt{\{1 + (1/K')\}\{(aI_0)/(b\beta)\} - V_{in}^2}}{\{1 + (1/K')\}^2}$$

$$+ \frac{2\{1 - (1/k')\}b\beta\, V_{in}^2}{\{1 + (1/K')\}^2}\, sgn\ (\ V_{in}\ ) \qquad (33\text{-}2)$$

$$+ \frac{2(1/K')}{\{1 + (1/K')\}} I_0\ sgn\,(\,V_{in}\,)$$

$$(\sqrt{(aI_0)/(K'b\beta)} \leq |V_{in}| \leq \sqrt{(aI_0)/(b\beta)})$$

$$\Delta I_2 = 2aI_0\ sgn(V_{in})\ (|V_{in}| \geq \sqrt{aI_0/(b\beta)}) \qquad (33\text{-}3)$$

$$\frac{d(\Delta I_2)}{dV_{in}} = \frac{8K'\sqrt{ab\beta I_0}}{(K'+1)\sqrt{1+K'}} \left[ \sqrt{1-\left[V_{in}^2 \Big/ \left[\{1+(1/K)\}\{(aI_0)/(b\beta)\}\right]\right]} - \frac{V_{in}^2/\left[\{1+(1/K')\}\{(aI_0)/(b\beta)\}\right]}{\sqrt{1+\left[V_{in}^2/\{1+(1/K')\}\{(aI_0)/(b\beta)\}\right]}} \right] \quad (34\text{-}1)$$

$$\left(|V_{in}| \le \sqrt{(aI_0)/(Kb\beta)}\right)$$

$$\frac{d(\Delta I_2)}{dV_{in}} = \frac{4K'\sqrt{ab\beta I_0}}{(K'+1)\sqrt{1+K'}} \left[ \sqrt{1-\left[V_{in}^2/\left[\{1+(1/K')\}\{(aI_0)/(b\beta)\}\right]\right]} - \frac{V_{in}^2/\left[\{1+(1/K')\}\{(aI_0)/(b\beta)\}\right]}{\sqrt{1+\left[V_{in}^2/\left[\{1+(1/K')\}\{(aI_0)/(b\beta)\}\right]\right.}} + \frac{4\{1-(1/K')\}b\beta V_{in}}{\{1+(1/K')\}^2} \right] \quad (34\text{-}2)$$

$$\left(\sqrt{(aI_0)/(Kb\beta)} \le |V_{in}| \le \sqrt{(aI_0/(b\beta)}\right)$$

$$\frac{d(\Delta I_2)}{dV_{in}} = 0 \quad (|V_{in}| \ge \sqrt{aI_0/(b\beta)}) \quad (34\text{-}3)$$

The differential output current $\Delta I$ of the differential amplifier circuit shown in Fig. 6 is given by $\Delta I = \Delta I_1 - \Delta I_2$, and its transconductance is given by $\{d(\Delta I)/dV_{in}\}$ as shown in the following expression (35).

$$d(\Delta I)/dV_{in} = \{d(\Delta I_1)/dV_{in}\} - \{d(\Delta I_2)/dV_{in}\} \quad (35)$$

Fig. 7 shows the transconductance characteristics thus obtained in which K, K', a and b are used as parameters. It is seen from Fig. 7 that the transconductance curve shows a ripple at its each side when K = 1.5, K' = 2.0, a = 0.387 and b = 0.478 in the input voltage range of $0.7(I_0/\beta)^{1/2} \ge |V_{in}|$. It is also seen from Fig. 7 that the transconductance curve shows an about 1.6 % ripple at its each side when K = 2.0, K' = 2.0, a = 0.473 and b = 0.739 in the input voltage range of $0.57(I_0/\beta)^{1/2} \ge |V_{in}|$.

Thus, the transconductance linearity of the differential amplifier circuit of the first embodiment can be drastically improved over the prior art.

In addition, it is seen from Fig. 7 that the current efficiency of the circuit can be increased.

With the second combined differential pair, in the first embodiment, the relative ratios of the transistors M5 and M6 and those of the transistors M7 and M8 are both K', their transconductance parameters are each b times as much as

those of the first combined differential pair, and the current values of the constant current sources 3 and 4 are a times as much as those of the constant current sources 1 and 2. However, these values of K7, a and b can be set appropriately to obtain various desired characteristics. For example, K' may be equal to K, or K' = K .

Fig. 8 shows a second differential amplifier circuit.

In Fig. 8, N-channel MOS transistors M1' and M2' compose a first differential pair which is driven by a constant current source 11 whose current value is $I_0$. N-channel MOS transistors M3' and M4' compose a second differential pair which is driven by a constant current source 12 whose current value is $I_0$.

A ratio (W/L) of a gate-width W and a gate-length L of the transistor M1' is equal to that of the transistor M2', and a ratio (W/L) of the transistor M3' is equal to that of the transistor M4'.

N-channel MOS transistors M5' and M6' compose a third differential pair which is driven by a constant current source 13 whose current value is $aI_0$ where $a \neq 1$. A ratio (W/L) of a gate-width W and a gate-length L of the transistor M5' is equal to that of the transistor M6' and is b times as much as that of the transistor M1' where $b \neq 1$.

As shown in Fig. 8, the transconductance parameters of the transistors M1' to M4' are equal to each other to be $\beta$, and those of the transistors M5' and M6' are b times as much as those of the transistors M1' to M4', or $b\beta$.

Gates of the transistors M1' and M5' are coupled together and gates of the transistors M4' and M6' are coupled together to form differential input ends. An input voltage $V_{in}$ is applied to the differential input ends thus formed.

Drains of the transistors M1', M3' and M6' are coupled together and drains of the transistors M2', M4' and M5' are coupled together to form differential output ends.

A first DC voltage $V_K$ is applied across the gates of the transistors M1' and M3' by a first DC voltage source 14, and a second DC voltage whose value is equal to that of the first DC voltage, or $V_K$, is applied across the gates of the transistors M2' and M4' by a second DC voltage source 15.

The polarity of the first DC voltage $V_K$ is made so that the voltage is high at the side of the transistor M3' and low at the side of the transistor M1'. The polarity of the second DC voltage $V_K$ is made so that the voltage is high at the side of the transistor M2' and low at the side of the transistor M4'.

Thus, in the first and second differential pairs, the DC voltages $V_K$ are applied as offset biases across the gates of the transistors M1' and M3' whose output ends are coupled together and the gates of the transistors M2' and M4' whose output ends are coupled together, respectively.

Next, the operation of the differential amplifier circuit is shown below.

The differential output current $\Delta I_1$ of the first differential pair is given as the following expressions (36-1), (36-2) and (36-3), the differential output current $\Delta I_2$ of the second differential pair is given as the following expressions (37-1), (37-2) and (37-3), and the differential output current $\Delta I_3$ of the third differential pair is given as the following expressions (38-1), (38-2) and (38-3).

$$\Delta I_1 = \beta (V_{in} + V_K) \sqrt{(2I_0/\beta) - (V_{in} + V_K)^2} \quad (|V_{in} + V_K| \leq \sqrt{I_0/\beta}) \tag{36-1}$$

$$\Delta I_1 = I_0 \quad (V_{in} + V_K \geq \sqrt{I_0/\beta}) \tag{36-2}$$

$$\Delta I_1 = -I_0 \quad (V_{in} + V_K \leq -\sqrt{I_0/\beta}) \tag{36-3}$$

$$\Delta I_2 = \beta (V_{in} - V_K) \sqrt{(2I_0/\beta) - (V_{in} - V_K)^2} \quad (|V_{in} - V_K| \leq \sqrt{I_0/\beta}) \tag{37-1}$$

$$\Delta I_2 = I_0 \quad (V_{in} - V_K \geq \sqrt{I_0/\beta}) \tag{37-2}$$

$$\Delta I_2 = -I_0 \quad (V_{in} - V_K \leq -\sqrt{I_0/\beta}) \tag{37-3}$$

$$\Delta I_3 = b\beta V_{in} \sqrt{(2aI_0)/(b\beta) - V_{in}^2} \quad (|V_{in}| \leq \sqrt{(aI_0)/(b\beta)}) \tag{38-1}$$

$$\Delta I_3 = I_0 \quad (V_{in} \geq \sqrt{(aI_0)/(b\beta)}) \tag{38-2}$$

$$\Delta I_3 = -I_0 \quad (V_{in} \leq -\sqrt{(aI_0)/(b\beta)}) \tag{38-3}$$

The differential output current of the differential amplifier circuit shown in Fig. 8 is given as the following expression (39).

$$\Delta I = \Delta I_1 + \Delta I_2 - \Delta I_3 \tag{39}$$

Differentiation of the differential output current $\Delta I$ by the input voltage $V_{in}$ leads to the transconductance of the differential amplifier circuit as shown in the following expressions (40).

$$d(\Delta I)/dV_{in} = \{d(\Delta I_1)/dV_{in}\} + \{d(\Delta I_2)/dV_{in}\} - \{d(\Delta I_3)/dV_{in}\} \quad (40)$$

Fig. 9 shows the transconductance characteristics thus obtained in which $V_K = (1/2)(I_0/\beta)^{1/2}$ and ab = 0.364333. It is seen from Fig. 9 that the transconductance fluctuation is restricted to 3 % or less in the input voltage range of $0.7(I_0/\beta)^{1/2} \geq |V_{in}|$, similar to the prior art.

The sum of the driving currents of the this embodiment is $(2 + a)I_0$ which is larger than that of $(1 + a)I_0$ of the prior-art differential amplifier circuit shown in Fig. 1. However, the differential output current of the this embodiment is $(2 - a)I_0$ which is also larger than that of $(1 - a)I_0$ of the circuit shown in Fig. 1. Therefore, the current efficiency of this embodiment is $\{(2 - a)/(2 + a)\}$ which is larger than that of $\{(1 - a)/(1 + a)\}$ of the circuit in Fig. 1.

For example, when a = 0.364, b = 1, the current efficiency of this embodiment is 0.692, and that of the prior-art circuit in Fig. 1 is 0.3423. This means that the current efficiency can be increased to about 2 times in current efficiency as much as the prior art in this embodiment.

As described above, the embodiment has the higher current efficiency than the first described embodiment together with the transconductance linearity similar to the prior art.

Fig. 10 shows a third differential amplifier circuit.

In Fig. 10, N-channel MOS transistors M1" and M2" compose a first differential pair which is driven by a constant current source 21 whose current value is $I_0$. A ratio (W/L) of a gate-width W and a gate-length L of the transistor M2" is K times as much as that of the transistor M1" where $K \neq 1$.

N-channel MOS transistors M3" and M4" compose a second differential pair which is driven by a constant current source 22 whose current value is $I_0$. A ratio (W/L) of the transistor M4" is K times as much as that of the transistor M3".

As shown in Fig. 10, the transconductance parameters of the transistors M1" and M3" are equal to each other to be $\beta$, and those of the transistors M2" and M4" are $K\beta$.

Gates of the transistors M1" and M4" are coupled together and gates of the transistors M2" and M3" are coupled together to form differential input ends. An input voltage $V_{in}$ is applied to the differential input ends thus formed.

Drains of the transistors M1" and M3" are coupled together and drains of the transistors M2" and M4" are coupled together to form differential output ends.

In the embodiment, said relative ratio K is set as 9.5, which is based on the following reason.

When all the transistors M1" to M4" are operating in their saturation regions, drain currents $I_{d1}$, $I_{d2}$, $I_{d3}$ and $I_{d4}$ of these transistors are respectively expressed as the following equations (41-1), (41-2), (41-3) and (41-4), where $V_{GS1}$, $V_{GS2}$, $V_{GS3}$ and $V_{GS4}$ are gate-to-source voltages of these transistors, respectively and $V_{TH}$ is the threshold voltage thereof.

$$I_{d1} = \beta(V_{GS1} - V_{TH})^2 \quad (41\text{-}1)$$

$$I_{d2} = K\beta(V_{GS2} - V_{TH})^2 \quad (41\text{-}2)$$

$$I_{d3} = K\beta(V_{GS3} - V_{TH})^2 \quad (41\text{-}3)$$

$$I_{d4} = \beta(V_{GS4} - V_{TH})^2 \quad (41\text{-}4)$$

Here, $I_{d1} + I_{d2} = I_{d3} + I_{d4} = I_0$ and $V_{GS1} - V_{GS2} = V_{GS4} - V_{GS3} = V_{in}$ are established, so that the difference $(I_{d1} - I_{d2})$ of the drain currents $I_{d1}$ and $I_{d2}$ is given as the following expressions (42-1), (42-2) and (42-3) and the difference $(I_{d3} - I_{d4})$ of the drain currents $I_{d3}$ and $I_{d4}$ is given as the following expressions (43-1), (43-2) and (43-3), respectively.

$$I_{d1} - I_{d2} = \frac{-\{1 - (1/K)\}[\{1 + (1/K)\}I_0 - 2\beta V_{in}^2]}{\{1 + (1/K)\}^2} + \frac{\beta V_{in}(4/\sqrt{K})\sqrt{\{1 + (1/K)\}(I_0/\beta) - V_{in}^2}}{\{1 + (1/K)\}^2} \quad (42\text{-}1)$$

$$\left(-\sqrt{I_0/\beta} \leq V_{in} \leq \sqrt{I_0/(K\beta)}\right)$$

$$I_{d1} - I_{d2} = I_0 \left(V_{in} \geq \sqrt{I_0/(K\beta)}\right) \quad (42\text{-}2)$$

$$I_{d1} - I_{d2} = -I_0 \ (V_{in} \leq -\sqrt{I_0/\beta}) \tag{42-3}$$

$$I_{d3} - I_{d4} = \frac{\{1-(1/K)\}\ [\{1+(1/K)\}I_0 - 2\beta V_{in}^2]}{\{1+(1/K)\}^2} + \frac{\beta V_{in}(4/\sqrt{K})\sqrt{\{1+(1/K)\}(I_0/\beta) - V_{in}^2}}{\{1+(1/K)\}^2} \quad \left(-\sqrt{I_0/(K\beta)} \leq V_{in} \leq \sqrt{I_0/\beta}\right) \tag{43-1}$$

$$I_{d3} - I_{d4} = I_0 \ (V_{in} \geq \sqrt{I_0/\beta}) \tag{43-2}$$

$$I_{d3} - I_{d4} = -I_0 \ (V_{in} \leq -\sqrt{I_0/(K\beta)}) \tag{43-3}$$

Accordingly, the differential output current of the differential amplifier circuit $\Delta I$ is given as the following expressions (44-1), (44-2) and (44-3), respectively. Then, differentiation of the differential output current $\Delta I$ by the input voltage $V_{in}$ leads to the transconductance of the differential amplifier circuit as shown in the following expressions (45-1), (45-2) and (45-3), respectively.

$$\Delta I = (I_{d1} + I_{d3}) - (I_{d2} + I_{d4}) \tag{44-1}$$

$$= (I_{d1} - I_{d2}) + (I_{d3} - I_{d4})$$

$$= \frac{(8/\sqrt{K})\ \beta V_{in}\sqrt{\{1+(1/K)\}(I_0/\beta) - V_{in}^2}}{\{1+(1/K)\}^2} \ (|V_{in}| \leq \sqrt{I_0/(K\beta)})$$

$$\Delta I = \frac{(4/\sqrt{K})\ \beta V_{in}\sqrt{\{1+(1/K)\}(I_0/\beta) - V_{in}^2}}{\{1+(1/K)\}^2} + \frac{2\{1-(1/k)\}\beta V_{in}^2}{\{1+(1/K)\}^2}\ sgn(V_{in}) + \frac{2\ (1/K)}{\{1+(1/K)\}}\ I_0\ sgn(V_{in}) \quad \left(\sqrt{I_0/(K\beta)} \leq |V_{in}| \leq \sqrt{I_0/\beta}\right) \tag{44-2}$$

$$\Delta I = 2I_0\ sgn(V_{in}) \ (|V_{in}| \geq \sqrt{I_0/\beta}) \tag{44-3}$$

$$\frac{d(\Delta I_1)}{d V_{in}} = \frac{8K\sqrt{\beta I_0}}{(K+1)\sqrt{1+K}} \left[ \sqrt{1-\left[V_{in}^2 / \left[\{1+(1/K)\}(I_0/\beta)\right]\right.} - \frac{V_{in}^2 / \left[\{1+(1/K)\}(I_0/\beta)\right]}{\sqrt{1+\left[V_{in}^2 / \{1+(1/K)\}(I_0/\beta)\right]}} \right] \quad (45\text{-}1)$$

$$\left(|V_{in}| \le \sqrt{I_0/(K\beta)}\right)$$

$$\frac{d(\Delta I_1)}{d V_{in}} = \frac{4K\sqrt{\beta I_0}}{(K+1)\sqrt{1+K}} \left[ \sqrt{1-\left[V_{in}^2 / \{1+(1/K)\}(I_0/\beta)\right]} - \frac{V_{in}^2 / \left[\{1+(1/K)\}(I_0/\beta)\right]}{\sqrt{1+\left[V_{in}^2 / \{1+(1/K)\}(I_0/\beta)\right]}} \right] + \frac{4\{1-(1/K)\}\beta V_{in}}{\{1+(1/K)\}^2} \quad (45\text{-}2)$$

$$\left(\sqrt{I_0/(K\beta)} \le |V_{in}| \le \sqrt{I_0/\beta}\right)$$

$$\frac{d(\Delta I_1)}{d V_{in}} = 0 \quad (|V_{in}| \ge \sqrt{I_0/\beta}) \quad (45\text{-}3)$$

When K = 9.5 is set in the expressions (45-1), (45-2) and (45-3), the transconductance curve of this embodiment has a ripple at each side and the best linearity of the transconductance can be obtained.

In the paper which discloses the prior-art differential amplifier circuit shown in Fig. 3, K is required to be set as 10 or more. However, it was found that this description is not correct and K = 9.5 is the best. Figs. 11 and 12 show the output characteristics and the transconductance characteristics, respectively.

It is seen from Fig. 12 that the transconductance fluctuation is restricted to -15 % or less in the input voltage range of $|V_{in}| \le 0.85 V_u$, where $V_u = (I_0/\beta)_{1/2}$. This means that the input voltage range which gives the transconductance having comparatively good linearity can be made wide sufficiently.

In a balanced differential pair formed of two transistors whose ratios (W/L) are equal to each other, in general, the transconductance fluctuation is about -30 % in the input voltage range of $|V_{in}| \le V_u$. Accordingly, it is seen that the transconductance linearity can be improved to 2 times as much as that of the circuit employing the balanced differential pairs by narrowing its input voltage range by about 15 %.

The condition of K = 9.5 can be realized with small gate sizes, or with restricting the transistor sizes, by the following method.

Similar to the prior-art differential amplifier circuit shown in Fig. 3, in the case that the gate-lengths of two MOS transistors forming an unbalanced differential pair are the same with each other and the gate-width of one of the transistor is K times as much as that of the other thereof, the sum $S_G$ of the gate areas of the two transistors is given as the following expression (46), where $S_{G1}$ and $S_{G2}$ are gate areas and $L_1$ and $L_2$, $W_1$ and $W_2$ are gate-lengths and gate-widths of these transistors, respectively.

$$S_G = S_{G1} + S_{G2} = L_1 W_1 (1 + K) \quad (46)$$

Contrary, in this embodiment, the ratios of the gate-length and gate-width of the transistors are defined as the following expressions (47-1) and (47-2), respectively considering the relative ratio of (W/L) is K.

$$W_1/L_1 = (1/K)^{1/2} \quad (47\text{-}1)$$

$$W_2/L_2 = K^{1/2} \quad (47\text{-}2)$$

Next, the minimum of the sum $S_G$ of the gate areas $S_{G1}$ and $S_{G2}$, which is given as the following expression (48), is obtained.

$$S_G = S_{G1} + S_{G2} = L_1W_1 + L_2W_2 \quad (48)$$

For example, in the case that the minimums of $L_1$ and $W_1$ are both 3μm, $S_G$ = 94.5 $\mu m^2$ from the expression (46) of the prior art and $S_G$ = 55.5 $\mu m^2$ from the expression (48) of this embodiment. This means that the sum of the gate areas in the embodiment can be reduced by 58.7%, which is equivalent to K = 5.2 in the prior art. As described above, K = 10 or more in the prior art as a result, it is seen that the transistor size can be reduced in the embodiment.

MOS transistors have comparatively large fabrication deviation, in general, so that the value of K deviates from the standard when K = 9.5. In other words, even if the value of K is set as 9.5, the value deviates from 9.5 to 9 or 10. The transconductance curves of K = 9.5, 9 and 10 are shown in Fig. 12, in which a curve of K = 9.5 is indicated by a solid line, that of K = 9 by a broken line and that of K = 10 by a chain line. However, since both transistors are used as a pair, variation of their characteristics can be restricted if both transistors made matched.

As described above, the sizes of the transistors M2" and M4" each having the larger ratio (W/L) of each differential pair can be restricted to several times as much as those of the transistors M1" and M3" having the smaller ratios (W/L) thereof. As a result, the circuit scale can be reduced. In addition, a transconductance with comparatively good linearity can be obtained in a wider input voltage range.

[First Embodiment]

Fig. 13 shows a differential amplifier circuit of a first embodiment, which is equivalent to that of the prior art shown in Fig. 4 in which a differential pair of transistors Q5 and Q6 driven by a constant current $aI_0$ is provided additionally.

In Fig. 13, NPN transistors Q1 and Q2 compose a first differential pair which is driven by a constant current source 31 whose current value is $I_0$. NPN transistors Q3 and Q4 compose a second differential pair which is driven by a constant current source 32 whose current value is $I_0$. NPN transistors Q5 and Q6 compose a third differential pair which is driven by a constant current source 33 whose current value is $aI_0$, where $a \neq 1$.

Bases of the transistors Q1 and Q5 are coupled together and bases of the transistors Q4 and Q6 are coupled together to form differential input ends. An input voltage $V_{in}$ is applied to the differential input ends thus formed.

collectors of the transistors Q1, Q3 and Q5 are coupled together and collectors of the transistors Q2', Q4' and Q6' are coupled together to form differential output ends.

A first DC voltage $V_K$ is applied across the bases of the transistors Q1 and Q3 by a first DC voltage source 34, and a second DC voltage whose value is equal to that of the first DC voltage, or $V_K$, is applied across the bases of the transistors Q2 and Q4 by a second DC voltage source 15.

The polarity of the first DC voltage $V_K$ is made so that the voltage is high at the side of the transistor Q3 and low at the side of the transistor Q1. The polarity of the second DC voltage $V_K$ is made so that the voltage is high at the side of the transistor Q2 and low at the side of the transistor Q4.

Thus, in the first and second differential pairs, the DC voltages $V_K$ are applied as offset biases across the bases of the transistors Q1 and Q3 whose output ends are coupled together and the bases of the transistors Q2 and Q4 whose output ends are coupled together, respectively.

Next, the operation of the differential amplifier circuit is shown below.

The operations of the first differential pair of the transistors Q1 and Q2 and the second differential pairs of the transistors Q3 and Q4 are the same as those in the prior art shown in Fig. 4 which are shown by the equations (17) to (25). Therefore, for the sake of simplification of description, only the operation of the third differential pair of the transistors Q5 and Q6 is described here.

The difference $\Delta I_3$ of collector currents $I_{C5}$ and $I_{C6}$ of the transistors Q5 and Q6 is given as the following expression (49) and its transconductance $G_{m3}$ is given as the following expression (50).

$$\Delta I_3 = I_{C5} - I_{C6} = \alpha_F\, aI_0 \tanh\{V_{in}/(2V_T)\} \quad (49)$$

$$G_{m3} = d(\Delta I_3)/dV_{in} = \{(\alpha_F\, aI_0)/(2V_T)\} \cdot [1/\{\cosh^2(V_{in}/2V_T)\}] \quad (50)$$

Therefore, the differential output current ΔI of the differential amplifier circuit of the fourth embodiment shown in Fig. 13 is given as the following expression (51), and then its transconductance $G_m$ is given as the following expression (52).

$$\Delta I = \Delta I_1 + \Delta I_2 + \Delta I_3 = \alpha_F I_0 [\tanh\{(V_{in}-V_K)/2V_T)\} + \tanh\{(V_{in}+V_K)/2V_T)\} + a \cdot \tanh(V_{in}/2V_T)] \quad (51)$$

$$G_m = G_{m1} + G_{m2} + G_{m3} = \frac{\alpha_F I_0}{2V_T} \left[ \frac{1}{\cosh^2\left(\frac{V_{in}-V_K}{2V_T}\right)} + \frac{1}{\cosh^2\left(\frac{V_{in}+V_K}{2V_T}\right)} + \frac{a}{\cosh^2\left(\frac{V_{in}}{2V_T}\right)} \right] \quad (52)$$

Fig. 14 shows the transconductance characteristics thus obtained in which $V_K = 2.634\ V_T$ and (1/a) = (4/3). It is seen from Fig. 14 that the transconductance curve shows a ripple of ±1 % or less at its each side is obtained and its fluctuation is limited to -1 % or less in the input voltage range of $|V_{in}| \leq 2.4\ V_T$.

Fig. 15 shows the transconductance characteristics in which $V_K = 2.06344\ V_T$ and (1/a) = 1.5625. It is seen from Fig. 15 that the transconductance curve having a maximally flat is obtained and its fluctuation is limited to -1 % or less in the input voltage range of $|V_{in}| \leq 1.3\ V_T$.

Thus, the transconductance linearity of the differential amplifier circuit of the first embodiment can be improved over the prior art and as a result, the input voltage range can be enlarged.

In addition, since each differential pair may be composed of two minimum unit transistors, its high-frequency characteristics can be improved.

[Second Embodiment]

Fig. 16 shows a differential amplifier circuit of a second embodiment, which is equivalent to that of two of the prior-art circuit shown in Fig. 4 are arranged together transversely.

In Fig. 16, NPN transistors Q1' and Q2' compose a first differential pair which is driven by a constant current source 41 whose current value is $I_0$. NPN transistors Q3' and Q4' compose a second differential pair which is driven by a constant current source 42 whose current value is $I_0$.

NPN transistors Q5' and Q6' compose a third differential pair which is driven by a constant current source 43 whose current value is $aI_0$ where $a \neq 1$. NPN transistors Q7' and Q8' compose a fourth differential pair which is driven by a constant current source 44 whose current value is $aI_0$.

Bases of the transistors Q1' and Q5' are coupled together and bases of the transistors Q4' and Q8' are coupled together to form differential input ends. An input voltage $V_{in}$ is applied across the differential input ends thus formed.

Collectors of the transistors Q1', Q3', Q5' and Q7' are coupled together and collectors of the transistors Q2', Q4' Q6' and Q8' are coupled together to form differential output ends.

A first DC voltage $V_{K1}$ is applied across the bases of the transistors Q1' and Q3' by a first DC voltage source 45, a second DC voltage whose value is equal to that of the first DC voltage, or $V_{K1}$, is applied across the bases of the transistors Q2' and Q4' by a second DC voltage source 46. A third DC voltage $V_{K2}$ is applied across the bases of the transistors Q5' and Q7' by a third DC voltage source 47, a fourth DC voltage whose value is equal to that of the third DC voltage, or $V_{K2}$, is applied across the bases of the transistors Q6' and Q8' by a fourth DC voltage source 48.

The polarity of the first DC voltage $V_{K1}$ is made so that the voltage is high at the side of the transistor Q3' and low at the side of the transistor Q1'. The polarity of the second DC voltage $V_{K1}$ is made so that the voltage is high at the side of the transistor Q2' and low at the side of the transistor Q4'. The polarity of the third DC voltage $V_{K2}$ is made so that the voltage is high at the side of the transistor Q7' and low at the side of the transistor Q5'. The polarity of the fourth DC voltage $V_{K2}$ is made so that the voltage is high at the side of the transistor Q6' and low at the side of the transistor Q8'.

Thus, in the first and second differential pairs, the first and second DC voltages $V_{K1}$ are applied as offset biases across the bases of the transistors Q1' and Q3' whose output ends are coupled together and the bases of the transistors Q2' and Q4' whose output ends are coupled together, respectively. Similarly, in the third and fourth differential pairs, the third and fourth DC voltages $V_{K2}$ are applied as offset biases across the bases of the transistors Q5' and Q7' whose output ends are coupled together and the bases of the transistors Q6' and Q8' whose output ends are coupled together, respectively.

Next, the operation of the differential amplifier circuit is shown below.

The current differences $\Delta I_1$, $\Delta I_2$, $\Delta I_3$ and $\Delta I_4$ of the first to fourth differential pairs are given as the following expressions (53-1), (53-2), (53-3) and (53-4), respectively.

$$\Delta I_1 = I_{C1} - I_{C2} = \alpha_F I_0 \tanh\{(V_{in}-V_{K1})/(2V_T)\} \quad (53\text{-}1)$$

$$\Delta I_2 = I_{C3} - I_{C4} = \alpha_F I_0 \tanh\{(V_{in}+V_{K1})/2V_T)\} \quad (53\text{-}2)$$

$$\Delta I_3 = I_{C5} - I_{C6} = a\alpha_F I_0 \tanh\{(V_{in}-V_{K2})/2V_T)\} \quad (53\text{-}3)$$

$$\Delta I_4 = I_{C7} - I_{C8} = a\alpha_F I_0 \tanh\{(V_{in}+V_{K2})/2V_T)\} \quad (53\text{-}4)$$

Therefore, the differential output current $\Delta I$ is given as the following expression (54), and then it transconductance $G_m$ is given as the following expression (55).

$$\Delta I = \Delta I_1 + \Delta I_2 + \Delta I_3 + \Delta I_4 \quad (54)$$
$$= \alpha_F I_0 \left[ \tanh\left(\frac{V_{in} - V_{K1}}{2V_T}\right) + \tanh\left(\frac{V_{in} + V_{K1}}{2V_T}\right) + a\left\{ \tanh\left(\frac{V_{in} - V_{K2}}{2V_T}\right) + \tanh\left(\frac{V_{in} + V_{K2}}{2V_T}\right)\right\}\right]$$

$$\frac{d(\Delta I)}{dV_{in}} = G_m = G_{m1} + G_{m2} + G_{m3} + G_{m4}$$
$$= \frac{\alpha_F I_0}{2V_T}\left[\frac{1}{\cosh^2\left(\frac{V_{in} - V_{K1}}{2V_T}\right)} + \frac{1}{\cosh^2\left(\frac{V_{in} + V_{K1}}{2V_T}\right)}\right. \quad (55)$$
$$\left. + \frac{a}{\cosh^2\left(\frac{V_{in} - V_{K2}}{2V_T}\right)} + \frac{a}{\cosh^2\left(\frac{V_{in} + V_{K2}}{2V_T}\right)}\right]$$

Fig. 17 shows the transconductance characteristics thus obtained in which $V_{K1} = 1.2\ V_T$, $V_{K2} = 3.834\ V_T$ and a = 1.3 in the expression (54). It is seen from Fig. 17 that the transconductance fluctuation is limited to -1 % or less in the input voltage range of $|V_{in}| \leq 3.5\ V_T$.

Fig. 18 shows the transconductance characteristics in which $V_{1K} = 0.70814\ V_T$, $V_{K2} = 2.59546\ V_T$ and a = 1.82532. It is seen from Fig. 18 that the transconductance curve having a maximally flat is obtained and its fluctuation is limited to -1 % or less in the input voltage range of $|V_{in}| \leq 1.9\ V_T$.

Thus, similar to the first embodiment, the transconductance linearity of the differential amplifier circuit of the second embodiment can he improved over the prior art and as a result, the input voltage range can be enlarged.

In addition, since each differential pair may be composed of two minimum unit transistors, its high-frequency characteristics can be improved.

## Claims

1. A differential amplifier circuit comprising:

a first differential pair formed of first and second transistors (Q1, Q2), which is driven by a first constant current source (31);

a second differential pair formed of third and fourth transistors (Q3, Q4), which is driven by a second constant current source (32) whose current value is equal to that of said first constant current source (31);

a third differential pair formed of fifth and sixth transistors (Q5, Q6), which is driven by a third constant current source (33) whose current value is different from those of said first and second constant current sources (31, 32);

bases of said first and fifth transistors (Q1, Q5) being coupled together and bases of said fourth and sixth transistors (Q4, Q6) being coupled together to form differential input ends; and

collectors of said first, third and fifth transistors (Q1, Q3, Q5) being coupled together and collectors of said second, fourth and sixth transistors (Q2, Q4, Q6) being coupled together to form differential output ends;

wherein a first DC voltage (34) is applied across said bases of said first and third transistors (Q1, Q3) and a second DC voltage (35) is applied across said bases of said second and fourth transistors (Q2, Q4); and

a polarity of said first DC voltage (34) with respect to said base of said first transistor (Q1) is the same as that of said second DC voltage (35) with respect to said base of said fourth transistor (Q4).

2. A differential amplifier circuit as claimed in claim 1, wherein values of said first and second DC voltages (34, 35) are both 2.634 $V_T$ where $V_T$ is the thermal voltage defined as $V_T = (k_B T/q)$ where $K_B$ is Boltzmann's constant, T is absolute temperature and q is the charge of an electron; and

values of said first and second constant current sources (31, 32) are both (4/3) times as much as that of said third constant current source (33).

3. A differential amplifier circuit as claimed in claim 1, wherein values of said first and second DC voltages (34, 35) are both 2.06344 $V_T$, where $V_T$ is the thermal voltage defined as $V_T = (k_B T/q)$ where $K_B$ is Boltzmann's constant, T is absolute temperature and q is the charge of an electron;

and values of said first and second constant current sources (31, 32) are both 1.5625 times as much as that of said third constant current source (33).

4. A differential amplifier circuit comprising:

a first differential pair formed of first and second transistors (Q1', Q2'), which is driven by a first constant current source (41);

a second differential pair formed of third and fourth transistors (Q3', Q4'), which is driven by a second constant current source (42) whose current value is equal to that of said first constant current source (41);

a third differential pair formed of fifth and sixth transistors (Q5', Q6'), which is driven by a third constant current source (43) whose current value is different from those of said first and second constant current sources (41, 42);

a fourth differential pair formed of seventh and eighth transistors (Q7', Q8'), which is driven by a fourth constant current source (44) whose current value is different from those of said first and second constant current sources (41, 42);

bases of said first and fifth transistors (Q1', Q5') being coupled together and bases of said fourth and eighth transistors (Q4', Q8') being coupled together to form differential input ends;

and collectors of said first, third, fifth and seventh transistors (Q1', Q3', Q5', Q7') being coupled together and collectors of said second, fourth, sixth and eighth transistors (Q2', Q4', Q6', Q8') being coupled together to form differential output ends;

wherein a first DC voltage (45) is applied across said bases of said first and third transistors (Q1', Q3'), a second DC voltage (46) is applied across said bases of said second and fourth transistors (Q2', Q4'), a third DC voltage (47) is applied across said bases of said fifth and seventh transistors (Q5', Q7'), and a fourth DC voltage (48) is applied across said bases of said sixth and eighth transistors (Q6', Q8'); and

a polarity of said first DC voltage (45) with respect to said base of said first transistor (Q1') is the same as that

of said second DC voltage (46) with respect to said base of said fourth transistor (Q4'), and a polarity of said third DC voltage (47) with respect to said base of said fifth transistor (Q5') is the same as that of said fourth DC voltage (48) with respect to said base of said eighth transistor (Q8').

5. A differential amplifier circuit as claimed in claim 4, wherein values of said first and second DC voltages (45, 46) are both 1.2 $V_T$ and those of said third and fourth DC voltages (47, 48) are both 3.834 $V_T$ where $V_T$ is the thermal voltage defined as $V_T = (k_B T/q)$ where $K_B$ is Boltzmann's constant, T is absolute temperature and q is the charge of an electron; and

values of said third and fourth constant current sources (43, 44) are both 1.3 times as much as those of said first and second constant current sources (41, 42).

6. A differential amplifier circuit as claimed in claim 5, wherein values of said first and second DC voltages (45, 46) are both 0.70814 $V_T$ and those of said third and fourth DC voltages (47, 48) are both 2.59546 $V_T$, where $V_T$ is the thermal voltage defined as $V_T = (k_B T/q)$ where $K_B$ is Boltzmann's constant, T is absolute temperature and q is the charge of an electron; and

values of said third and fourth constant current sources (43, 44) are both 1.82532 times as much as those of said first and second constant current sources (41, 42).

FIG. 1

PRIOR ART

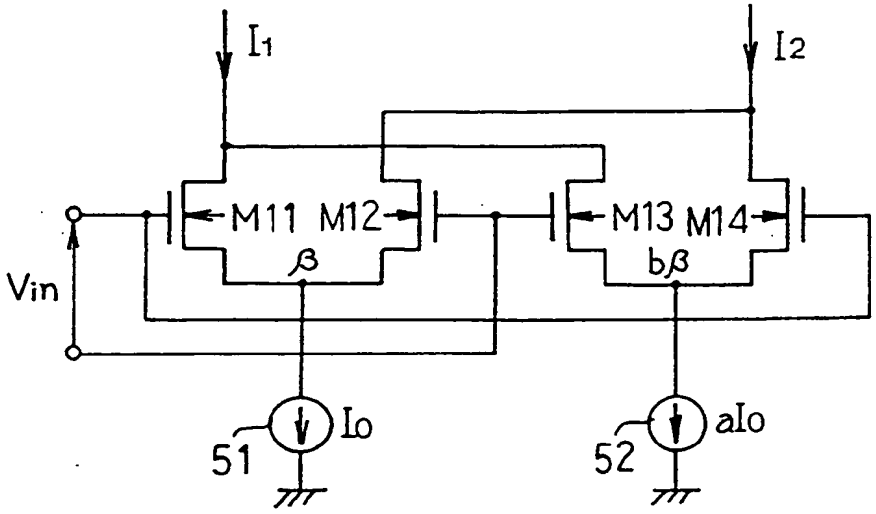



FIG. 3 PRIOR ART

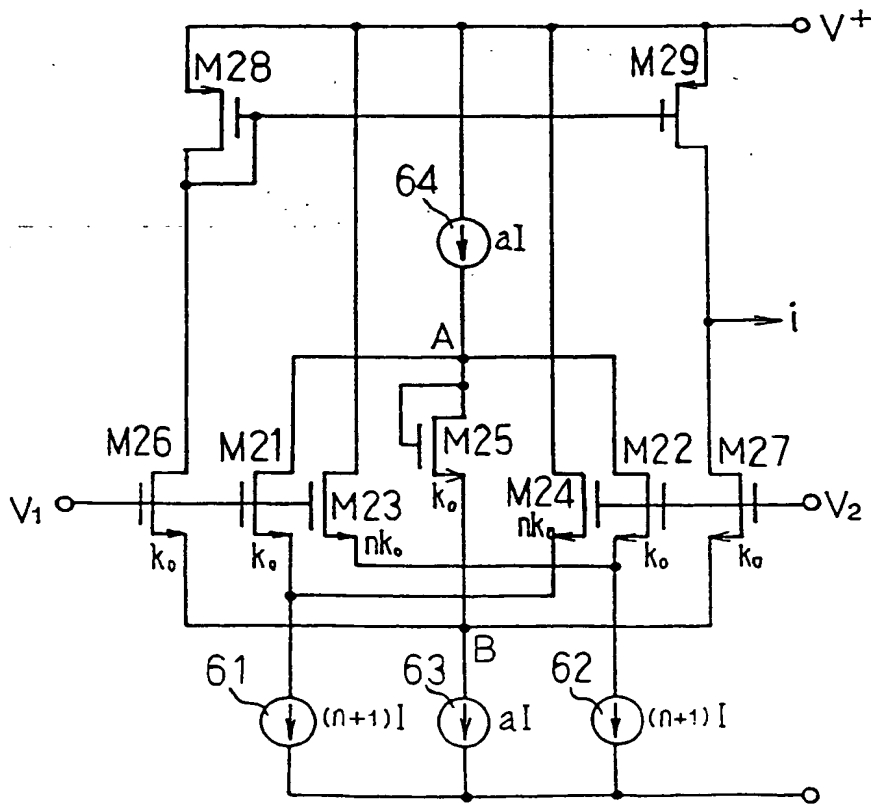


FIG. 2

PRIOR ART

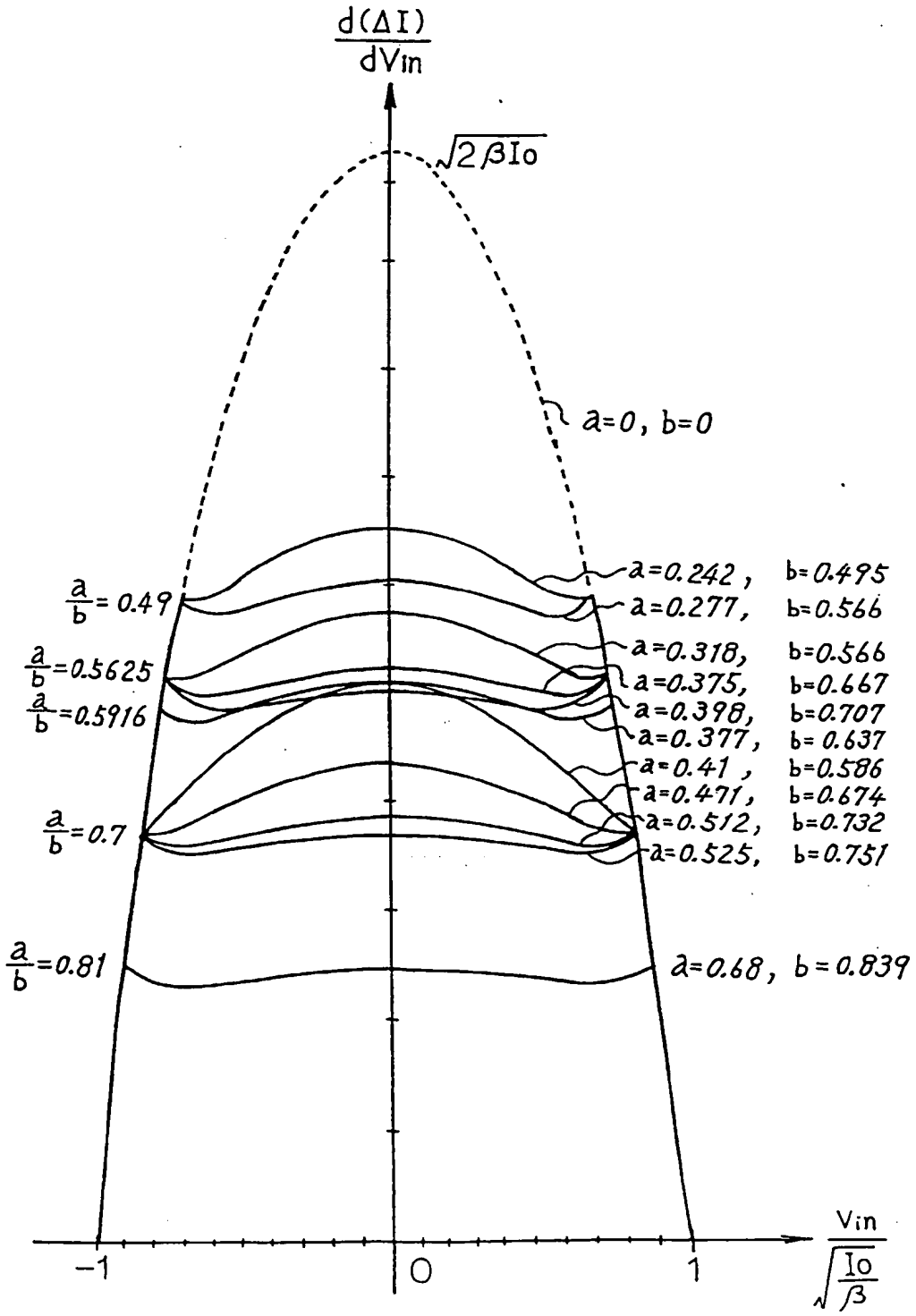


FIG. 4

PRIOR ART

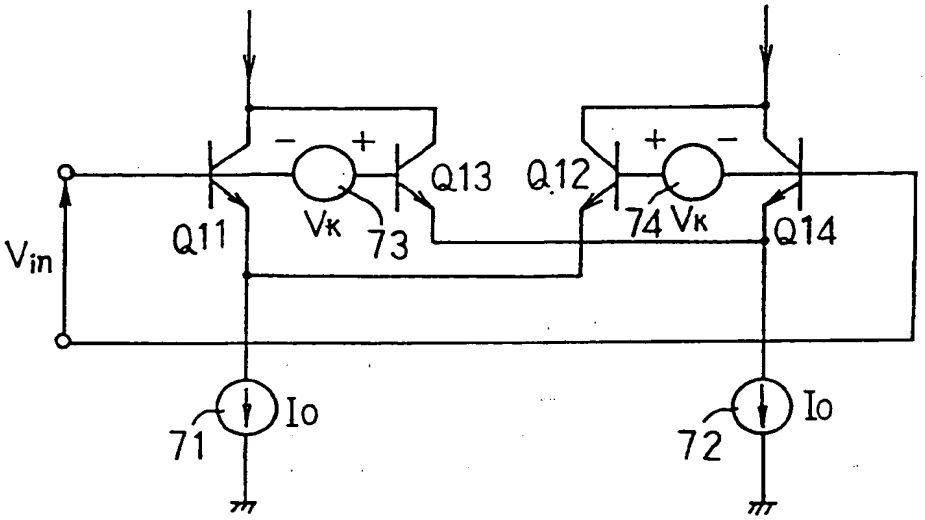



FIG. 5

PRIOR ART

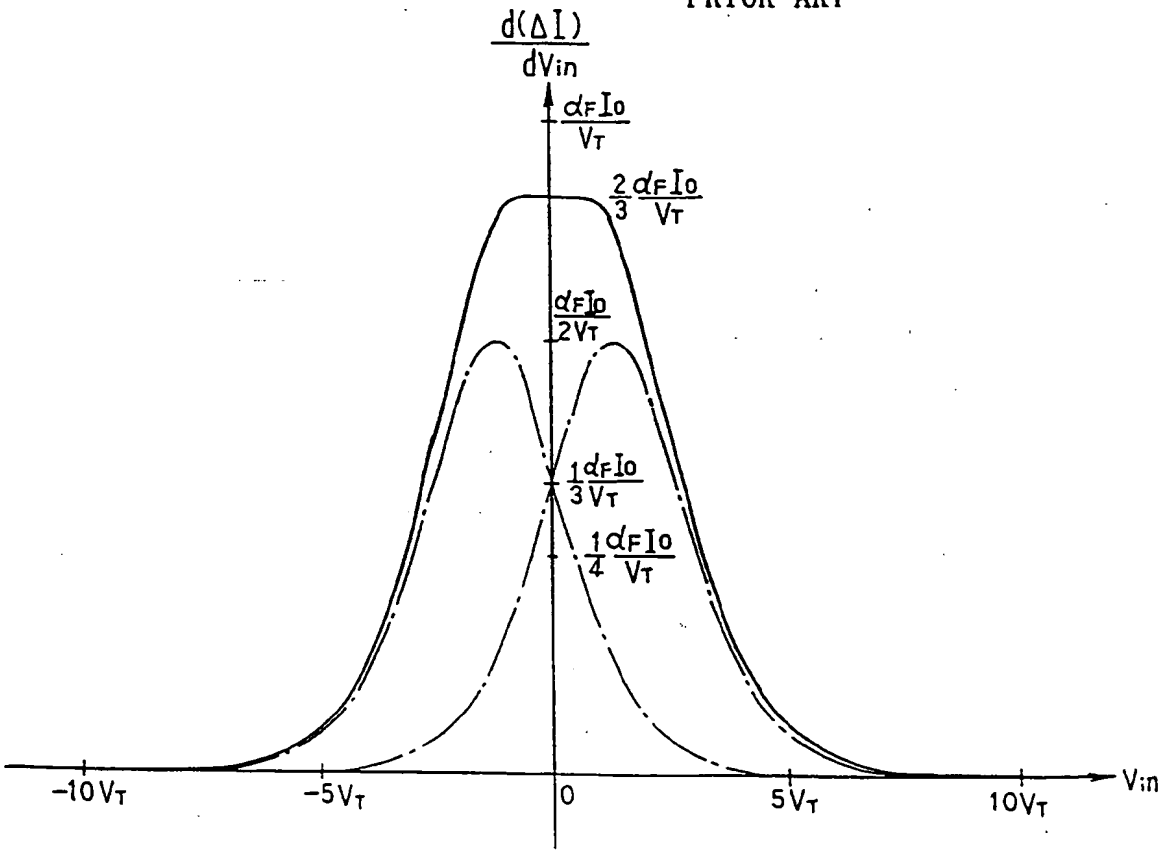


FIG. 6

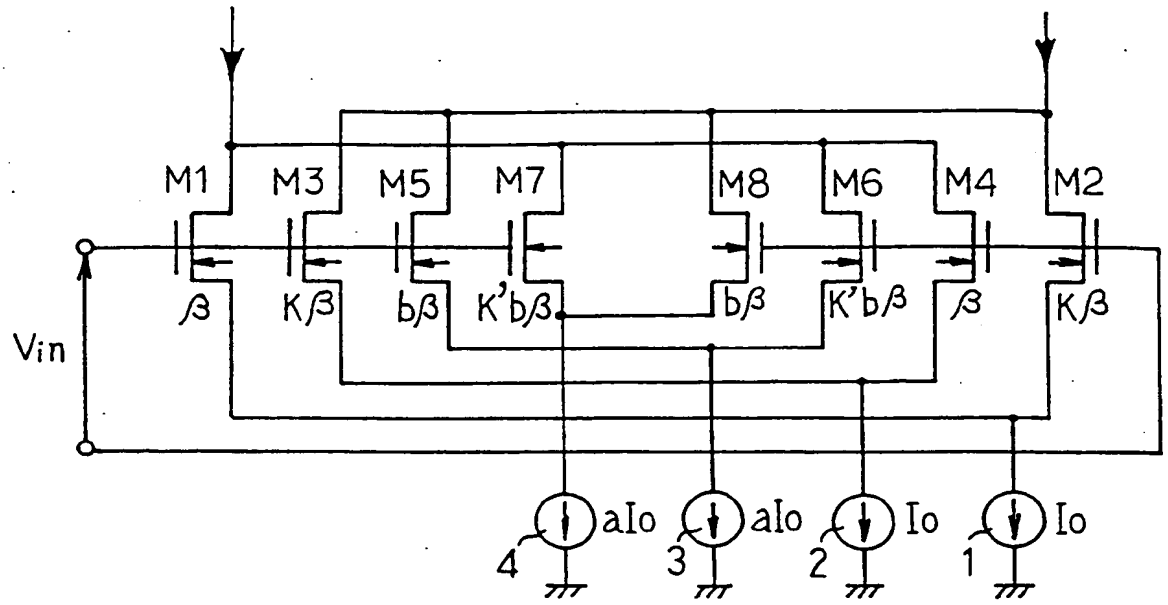



FIG. 8

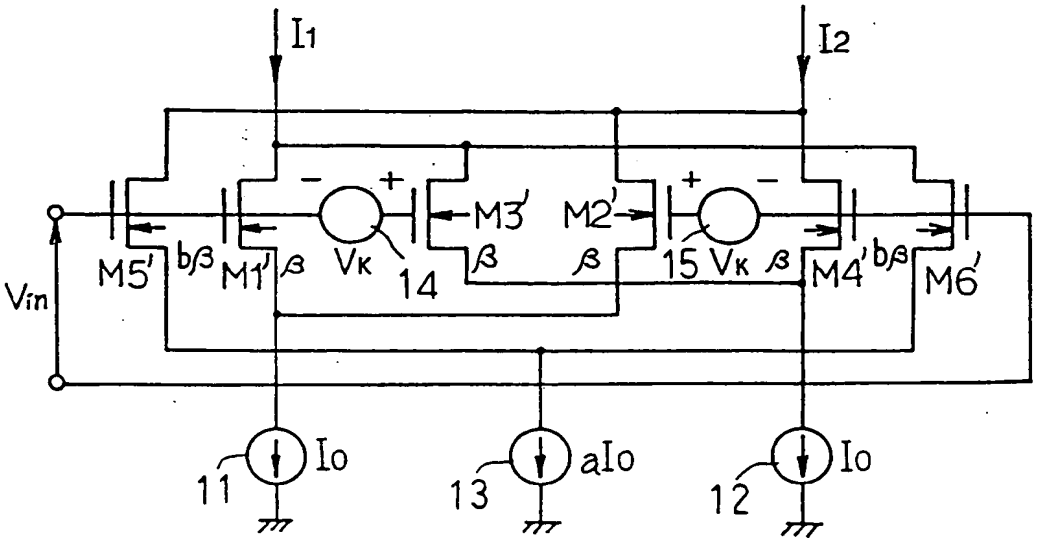


FIG. 7

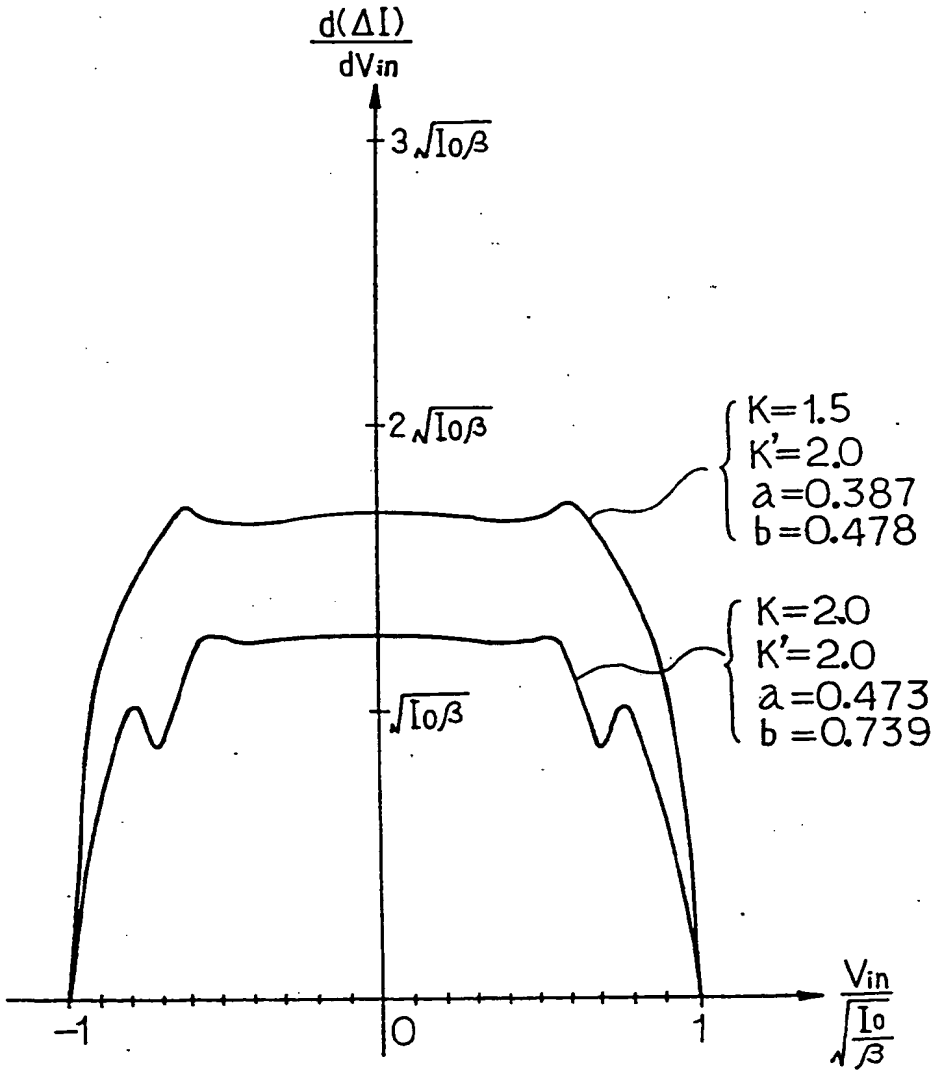

d(ΔI)
dVin
3√(Io/β)
2√(Io/β)
√(Io/β)
K=1.5
K'=2.0
a=0.387
b=0.478
K=2.0
K'=2.0
a=0.473
b=0.739
-1
0
1
Vin
√(Io/β)

FIG. 9

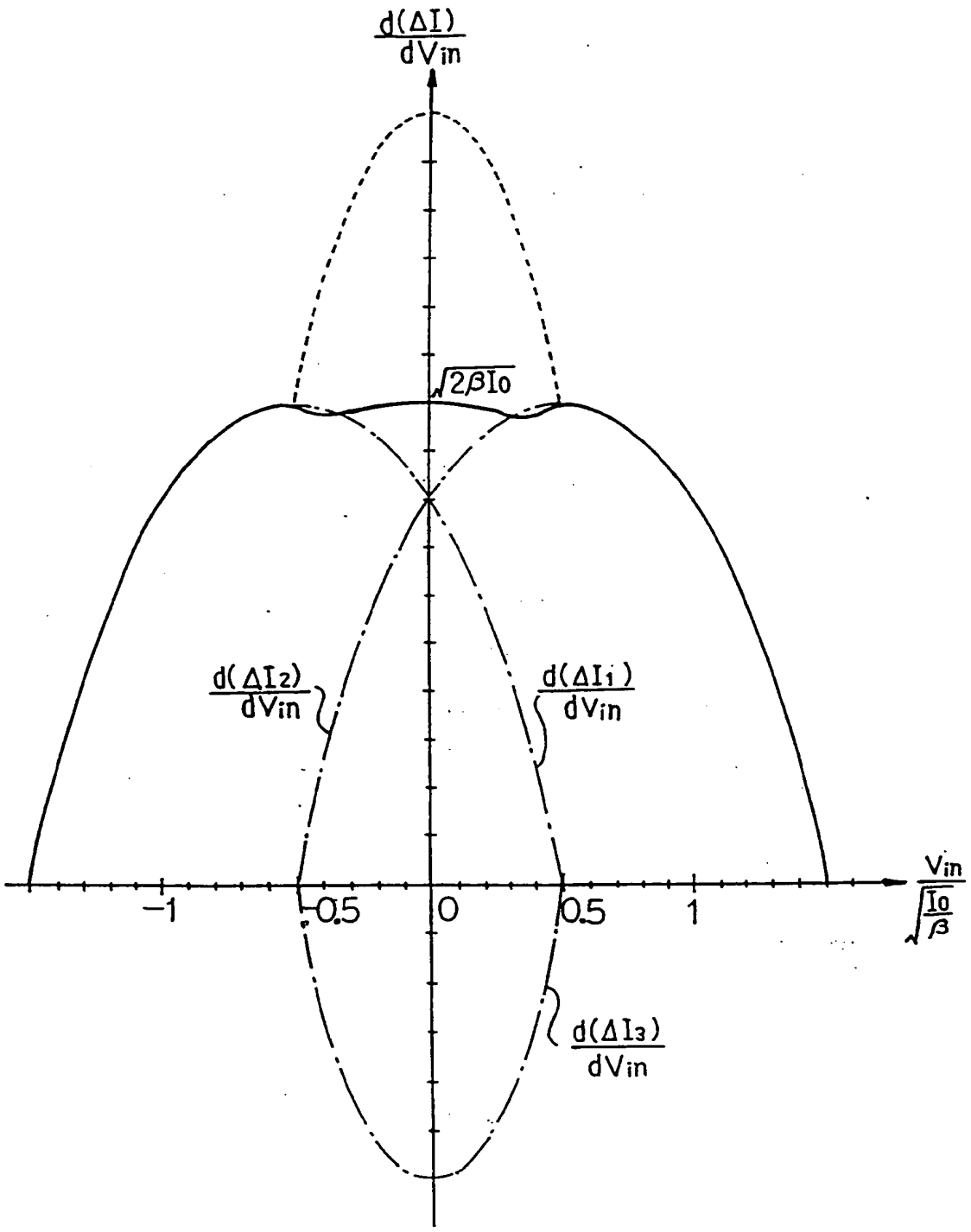


FIG. 10

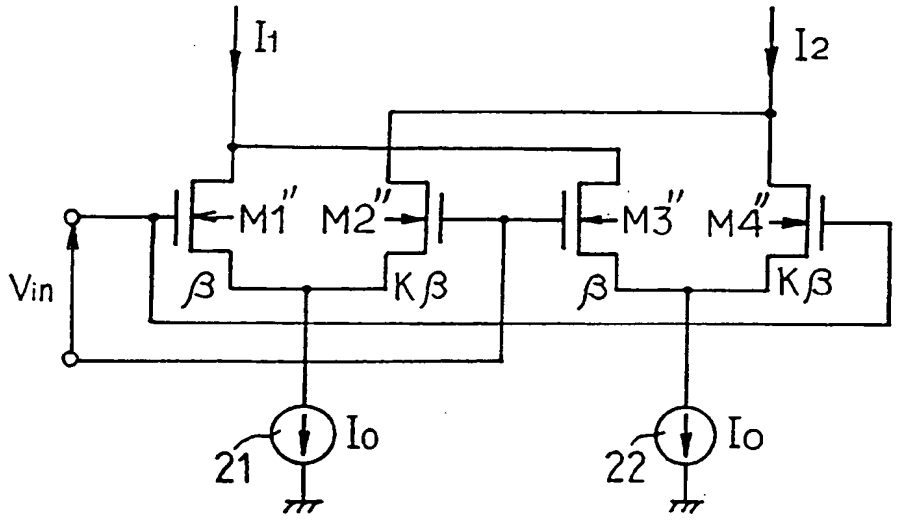

I1
I2
M1''
M2''
M3''
M4''
Vin
β
Kβ
β
Kβ
21
Io
22
Io

FIG. 13

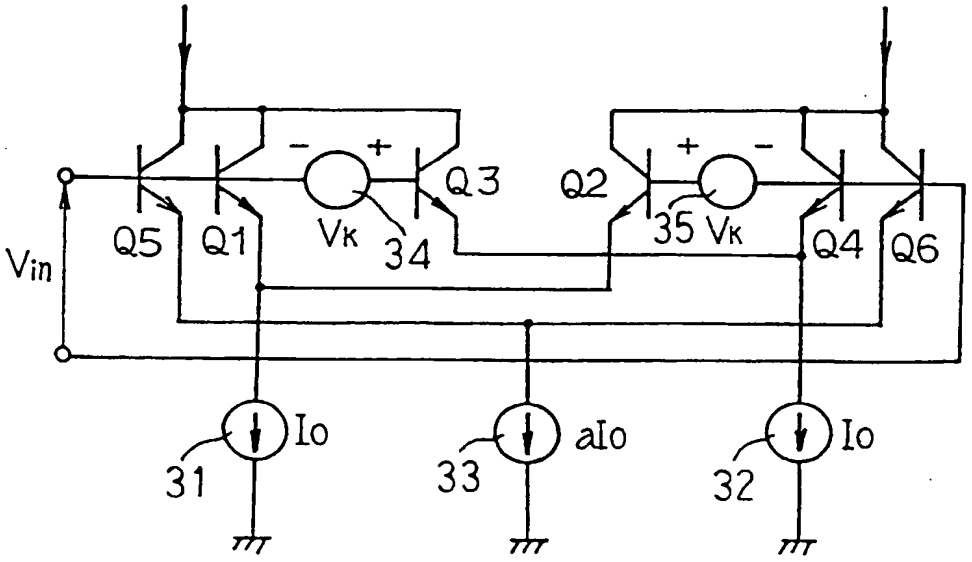

Q3
Q2
Q5
Q1
VK
34
35
VK
Q4
Q6
Vin
Io
31
aIo
33
Io
32

FIG. 11

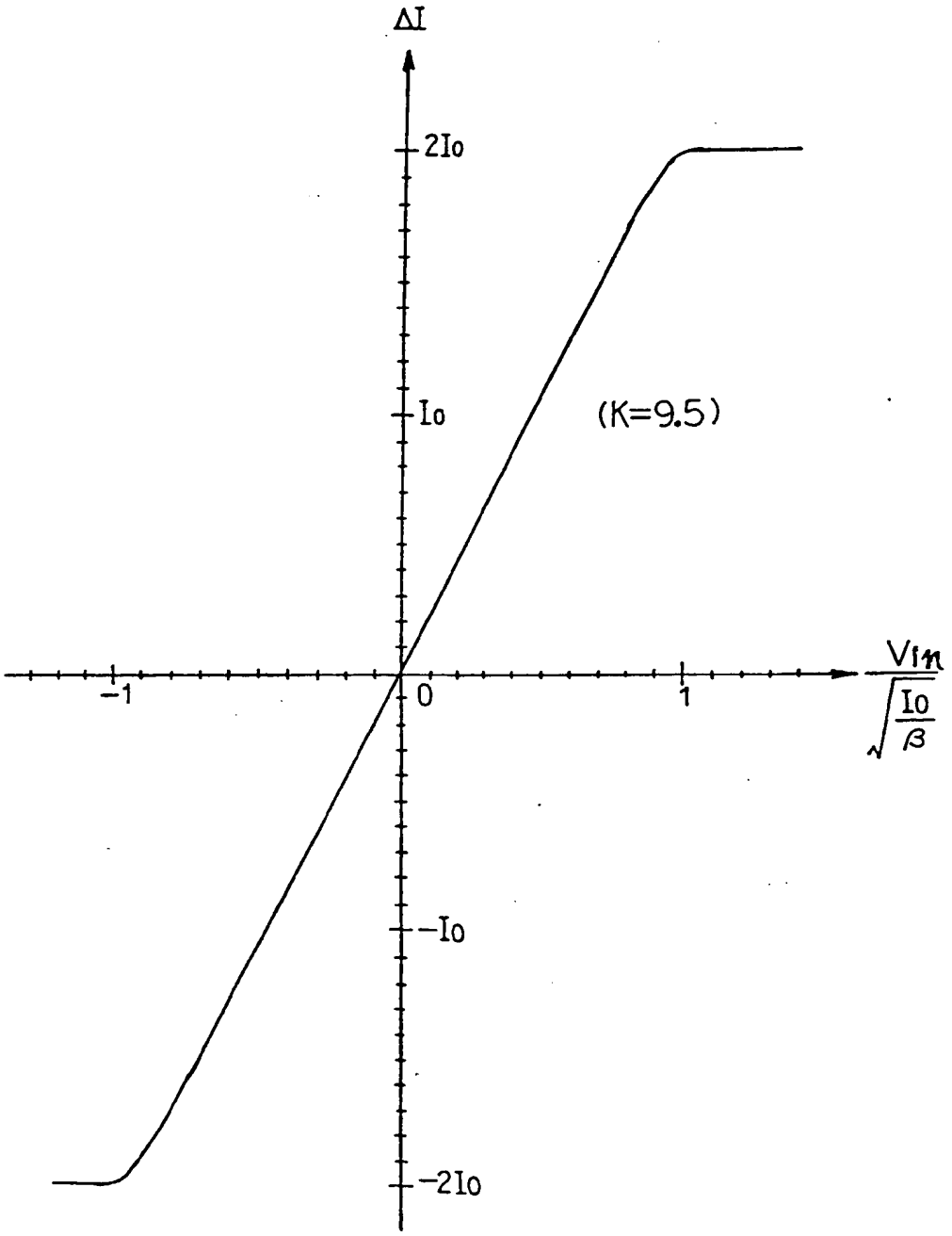


FIG. 12

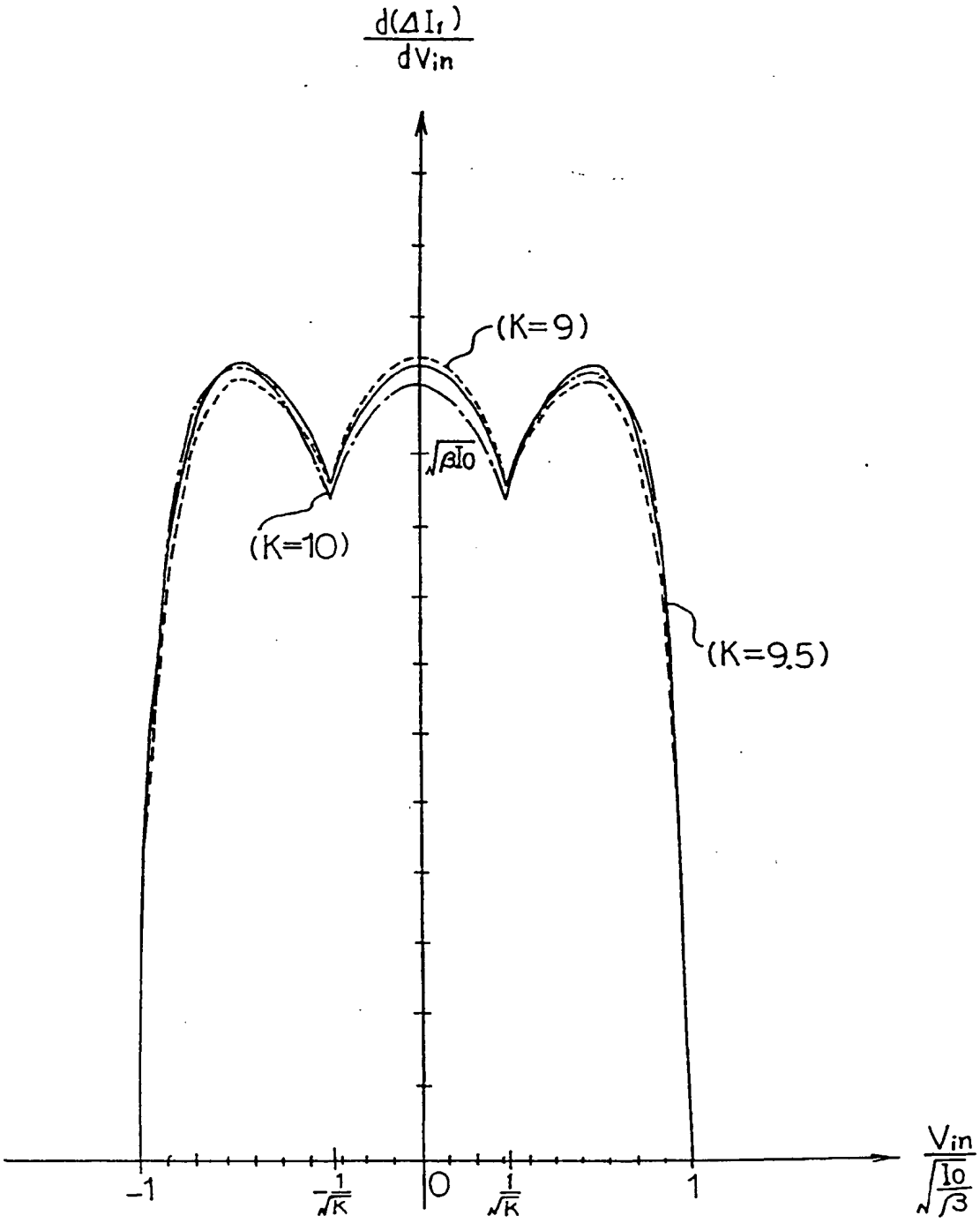


FIG. 14

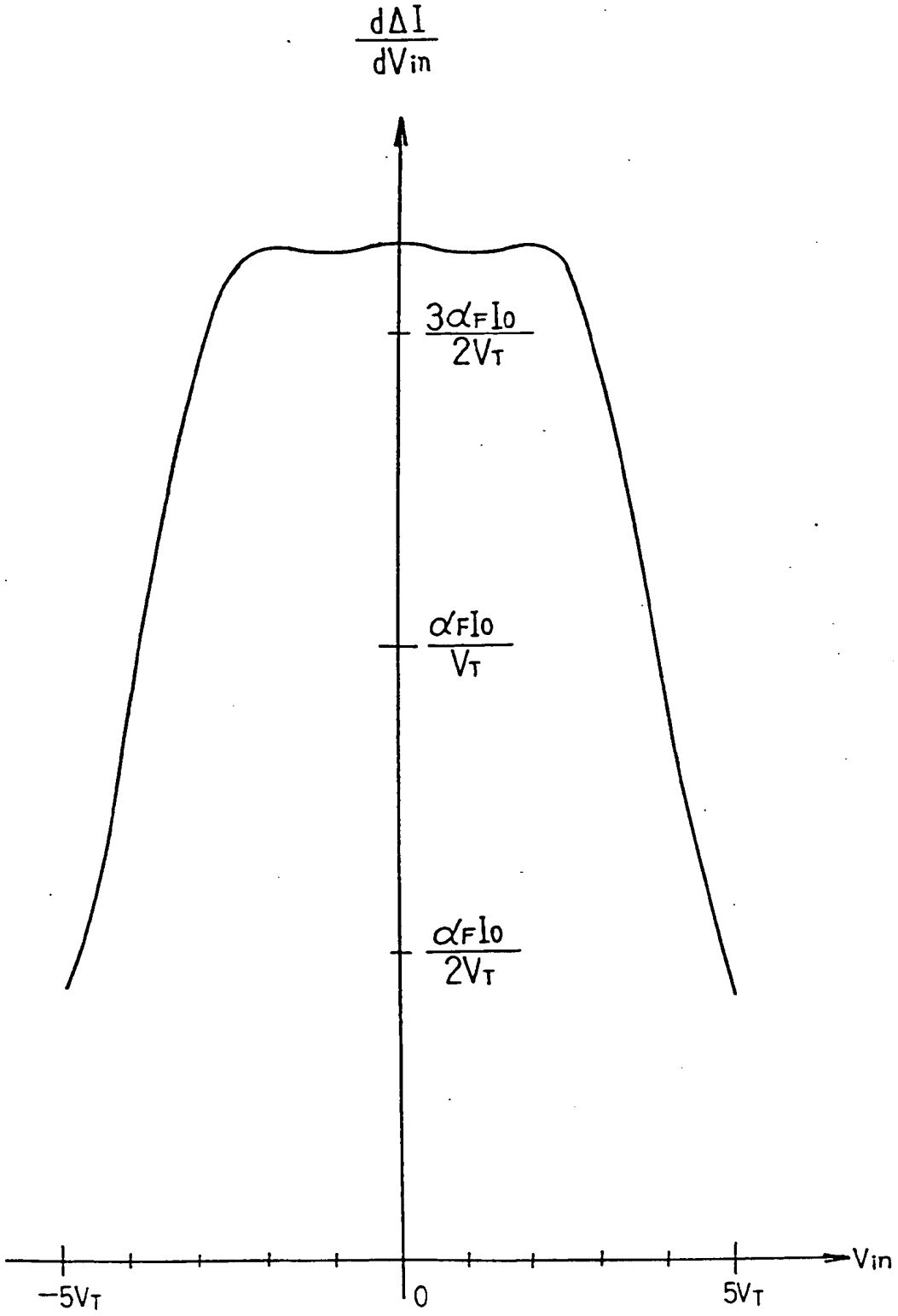


FIG. 15

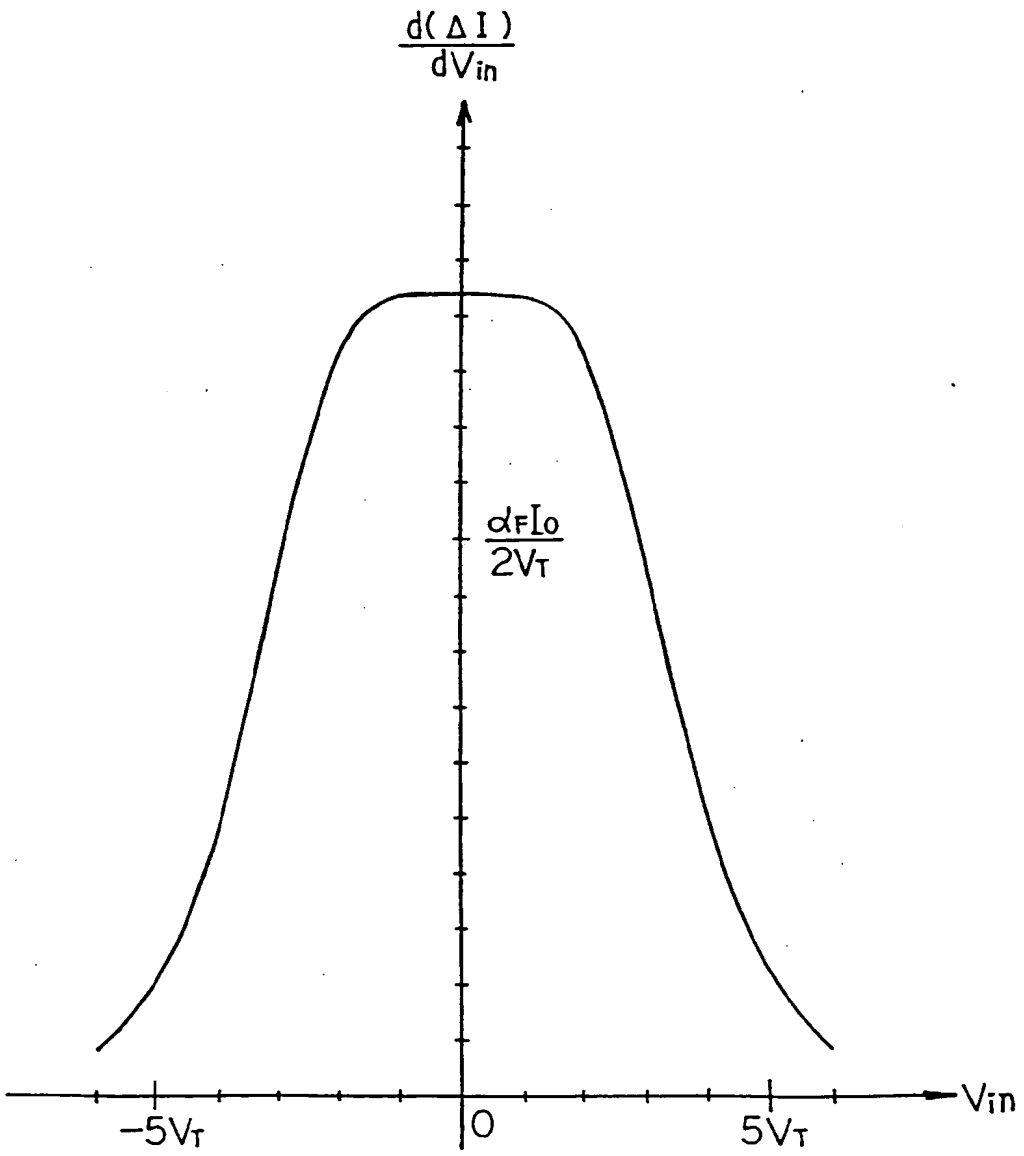


FIG. 16

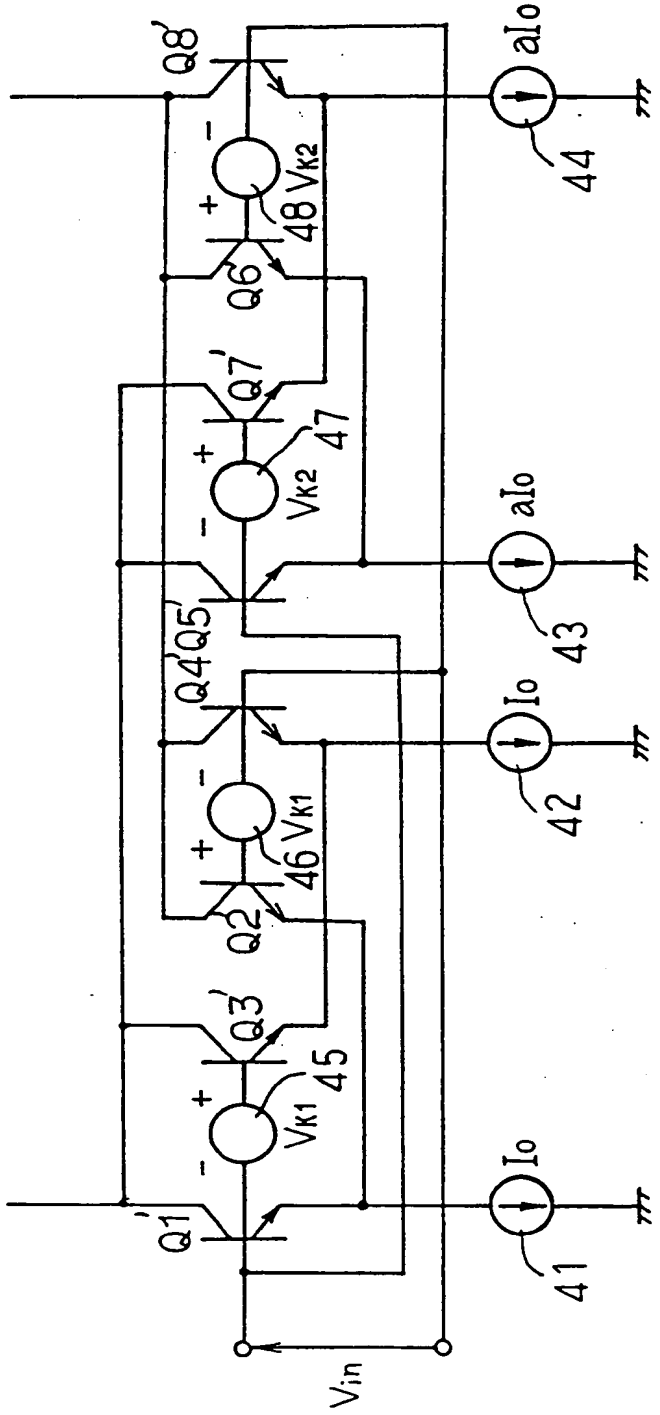


FIG. 17

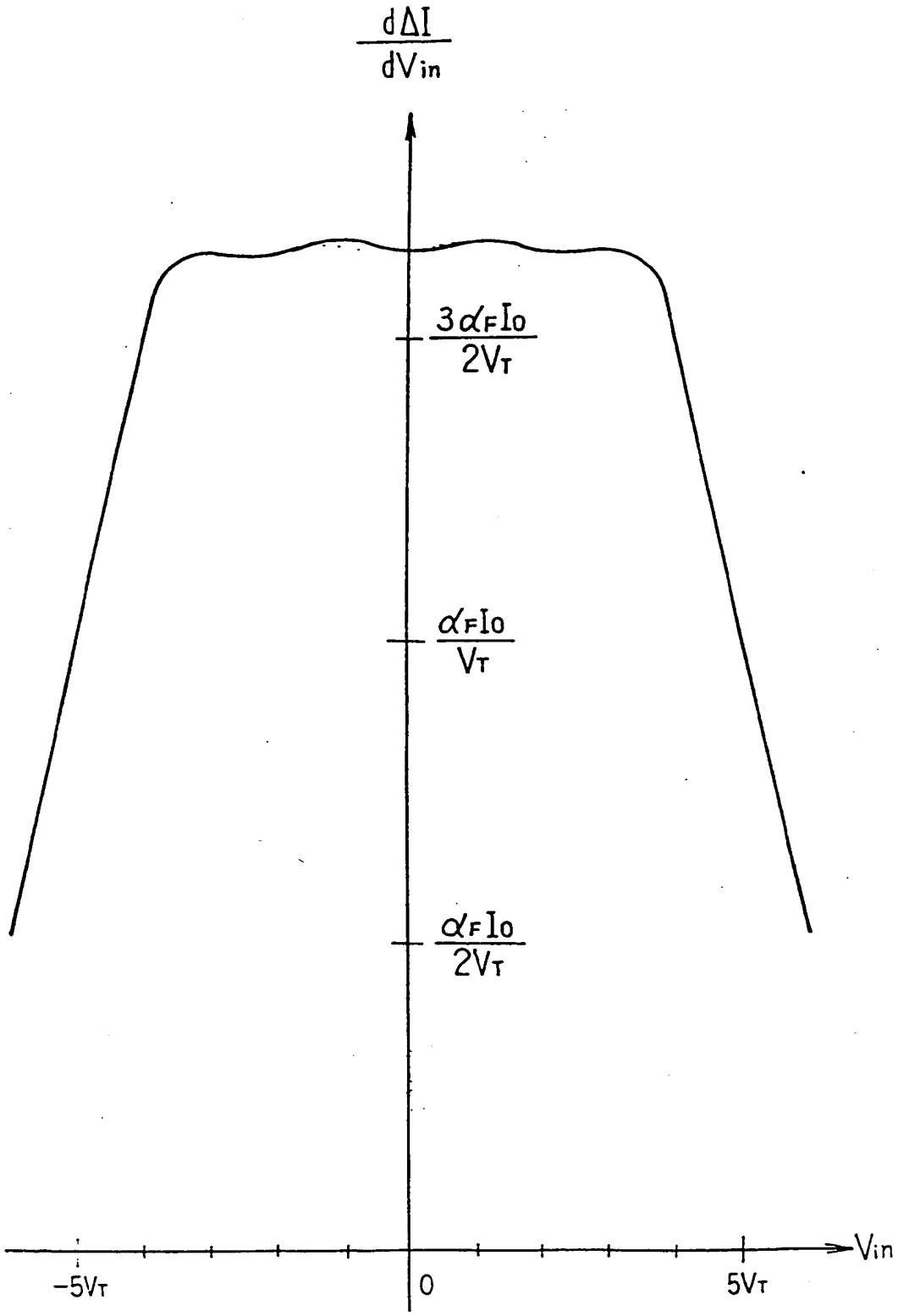
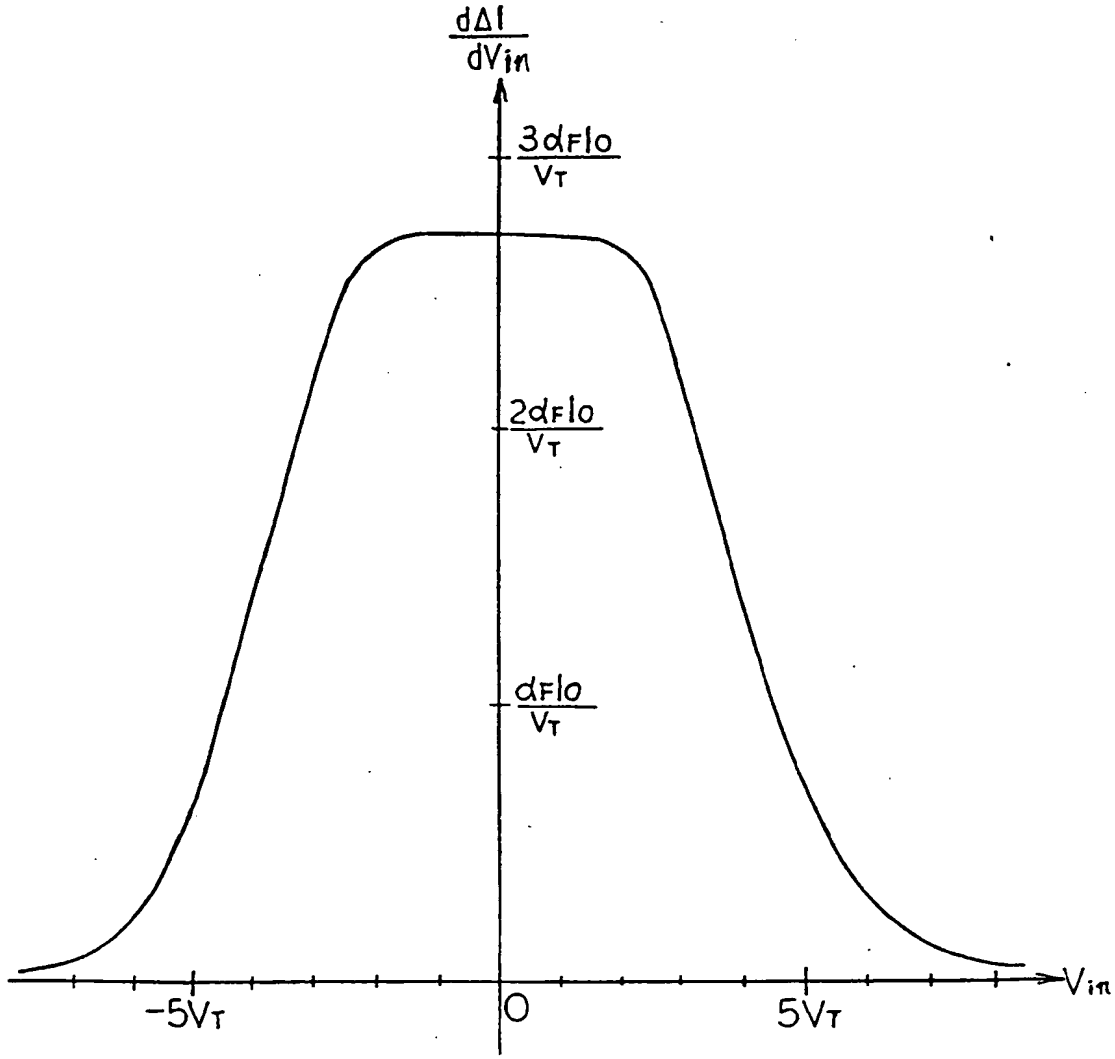


FIG. 18



(19) Europäisches Patentamt
Eur pean Patent Office
Office européen d s brevets

(11) EP 0 809 351 A3

# (12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
**04.03.1998 Bulletin 1998/10**

(43) Date of publication A2:
**26.11.1997 Bulletin 1997/48**

(21) Application number: **97113589.2**

(22) Date of filing: **08.12.1993**

(51) Int. Cl.[6]: **H03F 1/32**

(84) Designated Contracting States:
**DE FR GB IT NL SE**

(30) Priority: **08.12.1992 JP 351747/92**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
**93119773.5 / 0 601 560**

(71) Applicant: **NEC CORPORATION**
**Tokyo (JP)**

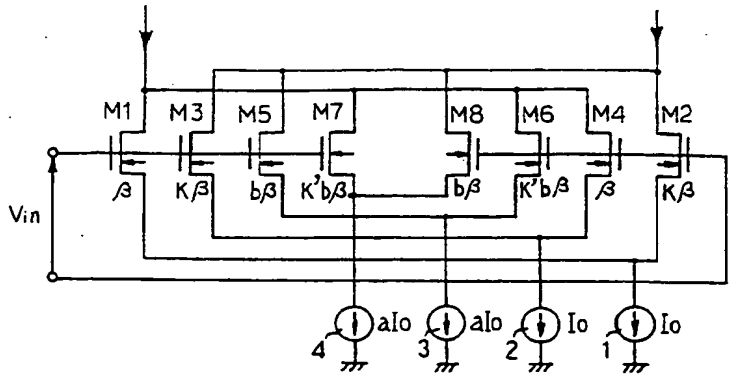
(72) Inventor: **Kimura, Katsuji**
**Minato-ku, Tokyo (JP)**

(74) Representative:
**VOSSIUS & PARTNER**
**Siebertstrasse 4**
**81675 München (DE)**

## (54) Differential amplifier circuit

(57) A differential amplifier circuit having an improved transconductance linearity, which includes a first to fourth unbalanced differential pairs of MOS transistors. In each differential pair, a ratio (W/L) of a gate-width W and a gate-length L of one transistor is different from that of the other transistor. Gates of the transistors having smaller ratios of the first and third pairs and gates of the transistors having larger ratios of the second and fourth pairs are coupled together to form one of differential input ends. Gates of the transistors having larger ratios of the first and third pairs and gates of the transistors having smaller ratios of the second and fourth pairs are coupled together to form the other of the input ends. Drains of the transistors having smaller ratios of the first and second pairs and drains of the transistors having larger ratios of the third and fourth pairs are coupled together to form one of differential output ends. Drains of the transistors having larger ratios of the first and second pairs and drains of the transistors having smaller ratios of the third and fourth pairs are coupled together to form the other of the output ends.

FIG. 6




EP 0 809 351 A3

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 97 11 3589

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| Y | EP 0 312 016 A (TOKYO SHIBAURA ELECTRIC CO)<br>* page 5, line 7 - line 35; figure 5 * | 1 | H03F1/32 |
| Y | DE 30 27 071 A (PHILIPS PATENTVERWALTUNG)<br>* page 8, line 17 - page 9, line 29; figure 1 * | 1 | |
| Y | HIROSHI TANIMOTO ET AL: "REALIZATION OF A 1-V ACTIVE FILTER USING A LINEARIZATION TECHNIQUE EMPLOYING PLURALITY OF EMITTER-COUPLED PAIRS"<br>IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 26, no. 7, 1 July 1991, pages 937-944, XP000237035<br>* page 938, paragraph A-D - page 939 * | 1,4 | |
| A,P | US 5 214 329 A (FURINO JR JAMES P)<br>* column 3, line 10 - line 50; figure 2 * | 1-3 | |
| Y | DE VEIRMAN G A ET AL: "DESIGN OF A BIPOLAR 10-MHZ PROGRAMMABLE CONTINUOUS-TIME 0.05 EQUIRIPPLE LINEAR PHASE FILTER"<br>IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 27, no. 3, 1 March 1992, pages 324-331, XP000295882<br>* page 326; figure 4 * | 4 | TECHNICAL FIELDS SEARCHED (Int.Cl.6)<br>H03F<br>H03H |
| A | KOYAMA, M. ET AL: "A 10.7 MHz continuous-time bandpass filter bipolar IC"<br>PROCEEDINGS OF THE IEEE 1989 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1989, NEW YORK USA, pages 25.2.1-25.2.4, XP002050487<br>* page 25.2.1 - page 25.2.3; figure 4 * | 1,4 | |

-/--

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 17 December 1997 | Breusing, J |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 97 11 3589

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| A | EP 0 352 009 A (SONY CORP)<br>* page 4, line 1 - line 46; figure 2 * | 1,4 | |
| A | GB 2 195 211 A (PLESSEY CO PLC)<br>* page 1, line 87 - line 130; figure 5 * | 1 | |
| A | US 4 460 872 A (MATTISSON SVEN)<br>* column 4, line 23 - line 65; figure 4 * | 1 | |
| A | GB 2 061 046 A (TOKYO SHIBAURA ELECTRIC CO)<br>* page 1, line 42 - page 3, line 31; figures 1,2 * | | |
| | | | TECHNICAL FIELDS SEARCHED (Int.Cl.6) |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 17 December 1997 | Breusing, J |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)